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INSTRUCTION MANUAL

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DAP SERIES
DIGITAL/ANALOG PROGRAMMER

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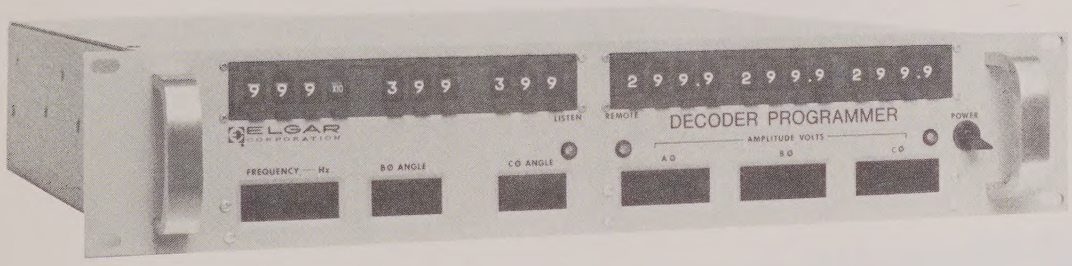

DAP SERIES
DIGITAL/ANALOG PROGRAMMER

104-DAP-XX/11-82/250

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SECTION I
GENERAL DESCRIPTION

1.1 INTRODUCTION

This instruction manual has been prepared for use with the Elgar series DAP Digital Decoder Programmer configured in accordance with information in Table 1.1.

The instructions contained herein are intended for use by systems engineers and by personnel responsible for the installation, operation and maintenance of the equipment. In addition to the information contained for a specific unit of the series DAP Digital Decoder Programmer, this manual contains some information of a more general nature relative to the entire DAP series. Because of the large number of options available, a single manual covering all possible combinations is not practical. However, it is appropriate to present a description of at least one of the more complex configurations where the installed options occupy all of the circuit board connectors and available front panel space. Such a system is described in this section and also in the functional description of Section IV, Theory of Operation.

1.2 General Description

The Elgar series DAP Digital Decoder Programmer is a solid state, self contained instrument intended for use in automatic test equipment (ATE) systems. In response to digitally coded address and command inputs from a central computer (controller) the DAP produces output signals that are, in turn, inputs to an AC Power Source and that determine the frequency, amplitude and phase of the power source outputs. Input options permit use of the standard IEEE-488 input or a 16 line, BCD coded and 6 line address input. Other options permit selection of fixed or programmable frequency, single, two or three phase outputs and, in the case of the two and three phase outputs, a fixed reference phase and one or two programmable phases.

Generally, the DAP will be remotely controlled. Local control, which may be selected remotely or with a front panel switch, is another option. It includes front panel mounted push-button rotary switches to control frequency, the phase angle of one or two outputs relative to the reference output, and the voltage output of each phase. When the optional, panel mounted LED command readouts are installed, the input command, from either the controller or the local function controls, will be displayed. The readouts are advantageous when troubleshooting the system, since they verify that the controller input signal has been received and properly decoded.

By providing the aforementioned options, Elgar is able to configure a DAP to meet the requirements of a wide spectrum of users.

The DAP utilizes input power of 117V AC (or 230V AC) over a frequency range of 47 Hz to 425 Hz. All internal power for the DAP is obtained from a single transformer, three rectifier systems and a number of voltage regulator circuits. Isolation is provided for the control input, power source driving signals and the local sense input. The chassis is connected to the ground pin of the 3-wire power connector, however, the internal

circuit grounds are isolated from the chassis and are common with the ground connection of the controller input. The output signals to the power source are isolated through individual transformers for each phase output and the sense inputs from the source load are also isolated through transformers mounted on the DAP chassis.

1.3 Physical Description

The DAP is housed in a rugged, all steel enclosure. The front panel is 3½ inches high and is designed for standard 19 inch rack mounting. The chassis of the instruments extends 17½ inches behind the mounting surface. The sides and top of the chassis are completely enclosed. Connectors for the controller input, output signals, as well as the primary power fuse holder, are mounted on the rear panel. The power cord, which enters the unit through the rear panel, is equipped with a 3-wire connector appropriate to the 117V or 230V power source to which it will be connected. A DAP without any of the front panel options will have a front panel mounted power switch and a "Power On" indicator. When the unit is equipped with the IEEE interface option, a "REMOTE" indicator, to show when the DAP is operating in the remote mode, and a "LISTEN" indicator, to show when it is receiving commands from the controller, will be installed on the front panel. The optional local function controls are in the form of pushbutton rotary switches that are mounted in two groups in a single row. A LOCAL/REMOTE switch will be installed on the front panel with this option, except in units with the IEEE interface option. When command LED readouts are installed, the display for each function is mounted behind a separate opening in the front panel. These openings are in a single row along the bottom of the panel. Two satin finished handles, for insertion and removal of the DAP from the mounting rack complete the front panel components. The customer may select the front panel color to harmonize with other instruments that may be mounted in the same equipment rack.

1.4 Instrument Identification

Because of the versatility of the Model DAP, the following is included to aid in the understanding of the significance of the characters in the complete model number embossed on the identification plate.

The "DAP" that appears as the first three characters of the model number merely denotes that the instrument is a digital decoder programmer. The number that appears immediately thereafter, (e.g., 1, 2 or 3) identifies the instrument as either a one, two or three phase device. Any one, or combination of, three letters may follow the model letters and phase identifiers and they have the following meanings:

A. The instrument is amplitude programmable.

F. The instrument is frequency programmable.

P. The instrument is phase programmable.

The numbers that follow the programmable identifiers indicate the options installed. These numbers will be found in the options list of Table 1.1.

1.5 Options

Because there are nine different options available for the Model DAP, the paragraphs that follow and that apply to your particular instrument should be reviewed.

1.5.1 Option 1, Parallel BCD Inputs, Positive True

Option 1 is a parallel, BCD 8421, positive true input to the DAP. The logic levels used in this option are 0.0 to +0.5VDC for a logic "0" and +2.5 to +5.0VDC for a logic "1". When Option 1 is incorporated, Option 3 may also be required to store the BCD pulse commands in the DAP if the Program Source (computer) is not configured such that the commands will be stored on the DAP input lines.

1.5.2 Option 2, Parallel BCD Inputs, Ground True

Option 2 is a parallel, BCD 8421, ground true

TABLE 1.1. OPTIONS LIST

Option 1: Logic "0" = 0V to +0.5V
Logic "1" = +2.5V to +5V

Option 2: Logic "0" = +2.5V to +5V
Logic "1" = 0V to +0.5V (ground true Logic)

Option 3: Internal Storage with Address Strobes for Options -1 or -2

Option -333: GPIB, IEEE-488-1975
The -333 option is in strict accordance with the IEEE-488-1975 as a LISTEN ONLY device. It's normal address is an ASCII-1 but other addresses can be set by an internal 5 gang DIP switch.

-4 Option: Analog Amplitude Modulation

-5 Option: Front Panel Local Control.

-6 Option: Front Panel Readouts.

-7 Option: 200V Bit. Provides the capability of amplitude programming from 0-260V in 0.2V steps.

-8 Option: Independent Amplitude Programming (multiphase systems only). Provides the capability of programming each phase independently or simultaneously.

input to the DAP. The logic levels used in this option are +2.5 to +5VDC for a logic "0" and 0.0 to +0.5VDC for a logic "1". When Option 2 is incorporated, Option 3 may also be required to store the BCD pulse commands in the DAP if the Program Source (computer) is not configured such that the commands will be stored on the DAP input lines.

1.5.3 Option 3, BCD Storage

Option 3 provides the necessary storage capability required if BCD pulses are used to program the DAP. The storage circuits are on the plug-in logic circuit cards. As many as six may be installed in the DAP, one for frequency, two for phase angle programming and three for amplitude programming. The DATA appearing on the 16 BCD input lines will be stored when the STROBE line for an individual circuit card goes true (+2.5 to 5 VDC for -1 logic or 0VDC for -2 logic). Overlapping DATA and STROBE commands are required to change a word in the storage. The DATA command should be 100 usec in duration and the STROBE command 50 usec in duration. These can be reduced to 20 usec and 10 usec, respectively. The overlapping commands minimize output voltage fluctuations during a programmed change. Each BCD storage card has capacity for storing 16 bits of command data. The BCD storage cards are interchangeable from one position to another.

1.5.4 Option 4, External Amplitude Modulation

Option 4 provides an external modulating input to the summing junction of the amplitude servo board. Modulation of the output is limited to 10% with an upper frequency limit of 9 Hz.

1.5.5 Option 5, Front Panel Local Control

Option 5 provides front panel mounted push-button rotary BCD switches for local control. This option may be incorporated for control of frequency, BØ and/or CØ phase angle programming, individual or simultaneous amplitude control of each phase. The local control switches may be incorporated for any of these functions in any combination.

1.5.6 Option 6, Front Panel Command Display

Option 6 provides panel mounted, command displays for each programmable function of the DAP. Thus, the commands for frequency, BØ and CØ phase angle and voltage amplitude of each phase will be displayed. Each display is comprised of 0.4 inch high, LED, seven-segment devices. The number of each device in each display is determined by the command resolution. The frequency display, therefore, is comprised of four digits. The phase angle displays are comprised of three digits and the amplitude displays are comprised of four digits. Displays will be installed for each programmable function when this option is specified. With this option installed, the command, whether generated locally or from the system programmer, will be displayed.

1.5.7 Option 7, 200V Bit

Option 7 enables the DAP to program the associated AC Power Source to 260V rather than the standard 130V.

1.5.8 Option 8, Independent Amplitude Programming

The Standard DAP, without Option 8 installed, programs all phases of multi-phase AC Power Source to the same output voltage. With Option 8 installed, each output may be independently programmed to any desired voltage level within the operating range.

1.5.9 Option -333, IEEE-488 Interface

Option -333 consists of a plug-in circuit board and an appropriate rear panel connector that will interface the DAP with a system controller (computer) operating in accordance with the Institute of Electrical Engineers (IEEE) Specification 488-1975. This option provides for parallel connection of all controlled devices within a system to a single bus. The DAP will then respond to commands from the controller after it has received a discrete, 5-bit address determined by the setting of a multiple switch assembly mounted on the IEEE Interface circuit board. The IEEE Interface converts the four-bit parallel, five-byte com-

mands from the controller to 16-bit, parallel commands compatible with the BCD storage capability of Option 3.

1.6 Specifications

The performance, mechanical and environmental specifications for the DAP are listed in Table 1.2.

1.7 Functional Description

A very simplified block diagram of a three-phase DAP (DAP-3) with frequency, phase angle and amplitude programming is shown in Figure 1.1. For simplicity, only the remote function is shown. This block diagram shows both the IEEE interface and the 16 bit BCD input. From the information presented in previous paragraphs, it will be obvious that only one of these inputs will be installed and in use. The data bus output of the IEEE interface is 16 lines coded in BCD. This is the same as the BCD input. The IEEE interface also generates a number of strobe pulses on individual lines, however, these are shown as a single line for simplicity. When the BCD input is used, the strobe signals are individually generated by the system controller. When command data on the bus is stabilized, a strobe pulse will load that data into the appropriate storage logic. The subsystem — frequency, phase angle or amplitude — will then respond to that input. The three-phase programmable oscillator has AØ, BØ and CØ outputs. However, the BØ and CØ outputs are not used in the system shown. The AØ and the DØ, which leads the AØ by 90^{o}, are used as inputs to the phase programmers. The phase programmers include two circuits to produce controlled amplitude outputs either in phase or 180^{o} out of phase, with their inputs. The outputs of these two circuits are combined in each programmer to produce an output which has the phase angle required to satisfy the input command. The AØ output from the oscillator and the outputs from the two phase programmers are then used as individual inputs to the three amplitude programmers. The programmers generate outputs, which drive the associated power source, that have the same phase as their input signals but the amplitude determined by the input commands. The sense inputs to the three amplitude programmers represent the voltage levels across the three legs of the load. These are compared in the amplitude programmers with the command input. Any difference between the command input and the voltage across the load produces an error voltage within the programmers to increase or decrease the source output to maintain the voltage across the load at the command level. The outputs of the amplitude programmers have an approximate range of 0 to 5V. Since the power source requires only 2V for full output, step down transformers are installed in the DAP between the output of the programmers and the inputs of the power source. Step down transformers are also inserted between the sense inputs and the input to the amplitude programmers. The ground returns of the output transformers are returned to the common connection of the power source. The ground returns of the sense transformers are returned to the common connection of the load. Thus, the transformers completely isolate the logic ground returns from those of the power source.

1.8 Auxiliary Equipment

The Elgar AC Power Sources, with which the DAP will be used, are designed for use with a plug-in oscillator. When the DAP is furnishing the frequency drive signal to the AC Power Source, the plug-in oscillator is removed. A signal routing plug-in which connects the Jones connector on the rear panel to the input of the amplifiers in the AC Power Source, is then installed in place of the oscillator. The plug-in configurations are required for different models of Elgar Power Sources are listed in Table 1.3.

TABLE 1.2. PERFORMANCE SPECIFICATIONS

STANDARD

INPUT POWER:
117 VAC ± 10%, 47-425 Hz single phase power, 100W maximum.
234 VAC ± 10%, 47-425 Hz single phase power, 100W maximum.

DIMENSIONS:
3.5" high, 16" deep and 19" wide. 25 lbs approximate weight.

SYSTEM SETTLING TIME:
100 ms. (includes power amplifier).

OUTPUT SIGNAL:
0.0 to 3v rms.

OPERATING TEMPERATURE RANGE:
0.0 to 50°C.

PROGRAMMING:
BCD 8421 (parallel entry) or IEEE-488.

FREQUENCY PROGRAMMING

FREQUENCY RANGE:
45 Hz to 10 KHz in 3 ranges; 45 Hz to 99.9 Hz in 0.1 Hz steps. 100 Hz to 999 KHz in 1.0 Hz steps. 1 KHz to 9.99 KHz in 10 Hz steps.

FREQUENCY ACCURACY:
±1% of programmed value.
±0.01% for fixed frequency.

FREQUENCY STABILITY:
±0.025% per °C maximum;
±0.25% for 24 hours at constant temperature.

PROGRAMMING TIME:
500 microseconds on any one range.

RANGE CHANGING TIME:
500 microseconds.

DISTORTION:
Less than 1% within power amplifier range.

TRANSIENT-FREE FREQUENCY:
No amplitude transient for frequency change on any one range.

FREQUENCY RESPONSE OF AMPLITUDE:
±0.1% of programmed value over 45-5 KHz range.

PHASE ANGLE PROGRAMMING

PHASE ANGLE RANGE:
0-359° in 1° steps relative to reference phase.

PHASE ANGLE ACCURACY:
±1° of programmed value from 45–1 KHz.

PHASE ANGLE STABILITY:
±0.25° for 24 hours at constant load and temperature.

TEMPERATURE COEFFICIENT:
±0.02 degree per °C average temperature coefficient.

PROGRAMMING TIME:
500 microseconds.

AMPLITUDE PROGRAMMING

VOLTAGE RANGES
A) 0.5V to 130V in 0.1V steps.
B) 0.5V to 260V in 0.1V steps with Option 7.

PROGRAMMING ACCURACY:
±0.25% of full scale value (Full Wave Average). Temperature range 0° to +55°C, warm-up 15 minutes.

LOAD REGULATION:
±0.01% (Full Wave Average) of programmed value at sense point.

LINE REGULATION:
±0.01% (Full Wave Average) of programmed value at sense point.

AMPLITUDE STABILITY:
±0.1% of programmed value for 1000 hours of constant line, load and temperature. Temperature coefficient ±0.005% per degree C average, 0° to +55°C.

PROGRAMMING TIME: (to 0.1% of programmed value)
0.5V to full output, less than 100 milliseconds; 10% to full output, less than 50 milliseconds; smaller steps proportionately less.

AMPLITUDE OVERSHOOT:
Less than 10%.

AMPLITUDE RESOLUTION:
100mv for 1V to 130V or 1V to 260V.

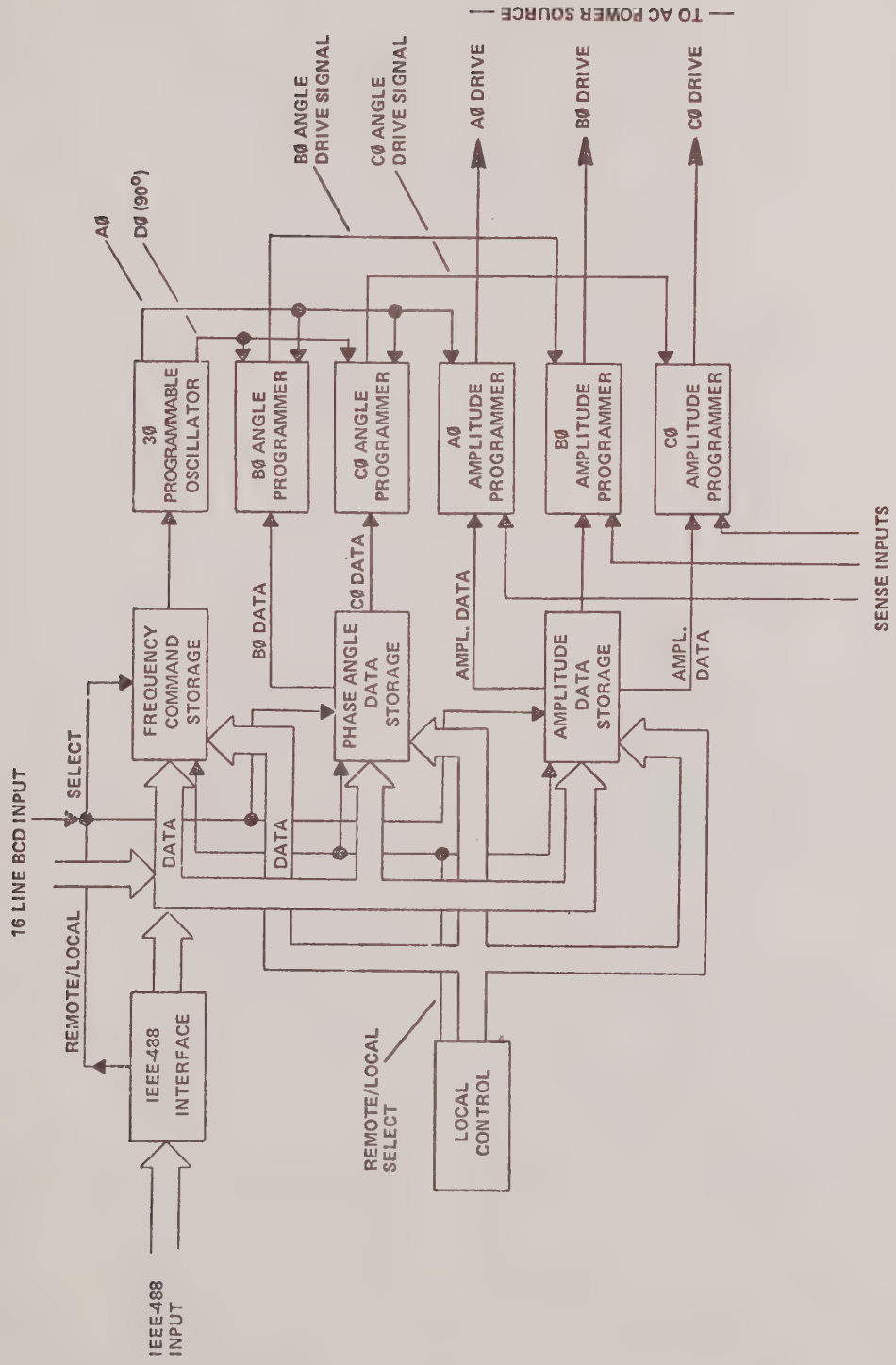


Figure 1.1. Simplified Block Diagram, DAP-3 Digital Decoder Programmer

TABLE 1.3. SIGNAL ROUTE PLUG-IN MODULES

Elgar AC Power Sources	400 SR Signal Routing Plug-Ins Configured as:
121	400-DPA
153B	400-DPA
251	400-DPA
501A	400-DPA
503A	400-DPA
751A	400-DPA
1001A	400-DPA
1751	400-DPA
1753A	400-DPA
3001	400-DPA

Elgar AC Power Systems	400 SR Signal Routing Plug-In Configured as:
360-3	400-DPA,B,C
750-3	400-DPA,B,C
1050-3	400-DPA,B,C
1500-3	400-DPA,B,C
2250-3	400-DPA,B,C
3000-3	400-DPA,B,C
5250-3	400-DPA,B,C
500-3D	400-DPA,400-DPB
1000-3D	400-DPA,400-DPB
2000-3D	400-DPA,400-DPB
3500-3D	400-DPA,B
500-2	400-DPA,400-DPB
1000-2	400-DPA,400-DPB
1000-1	400-DPA (2 pcs)
2000-1	400-DPA (2 pcs)

SECTION II
INSTALLATION

2.1 GENERAL

This section of the manual contains instructions for pre-installation inspection, mechanical installation and electrical connections.

2.2 Preinstallation Inspection

Because of the rugged construction of the Elgar DAP Digital Decoder Programmer, only extreme mishandling in transit should result in physical damage. Nevertheless, the equipment should be inspected on receipt. The preinstallation inspection consists of the following steps:

1. Inspect the instrument exterior for any signs of damage such as dents, scratches, or distortion.

2. All front panel controls should be checked for ease of operation and that there is no breakage.

3. Check the digital displays for breakage or misalignment.

4. Remove the top cover and verify that all circuit boards are firmly seated in their sockets. Also check the mother board for any evidence of cracks which might have been caused by mishandling during shipment.

5. Check the rear panel connectors for any evidence of damage or distortion.

6. Check that the power cord is securely attached where it enters the rear panel and that the power plug is undamaged.

NOTE

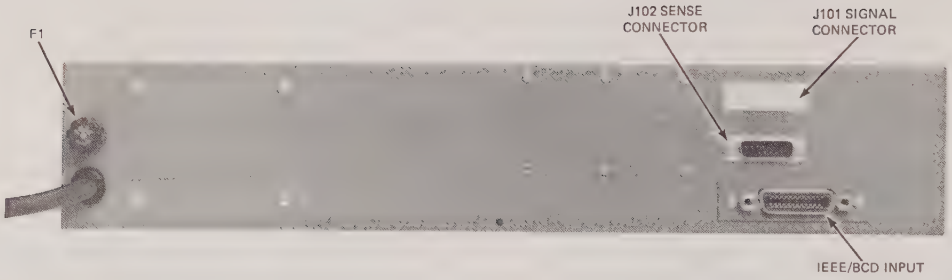
If damage is evident, save all shipping material and inform the carrier's agent immediately. Damaged equipment must not be returned to Elgar Corporation until the carrier's agent has approved repairs and until a return authorization has been obtained from Elgar Corporation. Forward a damage report to Elgar Service Department, 8225 Mercury Court, San Diego, California 92111. Elgar will then provide instructions for repair or replacement of the damaged instrument.

2.3 Rack Mounting

The Model DAP has been designed for rack mounting. Threaded holes on each side have been provided for installation of Zero Manufacturing Company slides, Model CTN-118. The external dimensions, and location of rear panel connectors, are shown in Figure 2.1. Follow Zero Manufacturing Company's instructions for attachment of the slides to the equipment rack.

2.4 Electrical Connections

On the assumption that the DAP will be installed in the same equipment rack as the power source, a two foot cable is provided with the DAP



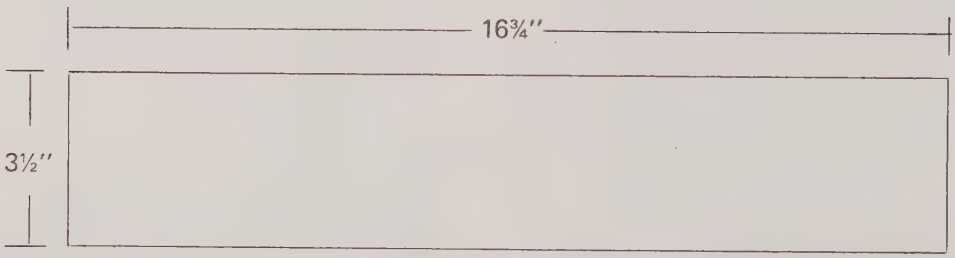


Figure 2.1. External Dimensions and Connector Data

for interconnecting the output of the DAP and the input of the power source. To install this cable, proceed as follows:

1. Connect the two-foot control cable from connector J101 on the rear of the DAP to connector J1 on the AC Power Source. If the power source is furnished by a manufacturer other than Elgar, refer to Figure 2.2 for the DAP output signal connections. The common connection of J101 should be directly connected to the common input connection of the power source.

2. Install the necessary wires on the remote sensing cable connector provided. Connect the wires from this connector to the power source output in accordance with the information of Figure 2.2. If appreciable voltage drop in the wiring between the power source output and the load is anticipated, it is advisable to connect the sense input leads to the load terminals. When the sense input leads are connected to the load terminals, their common connection should be connected to the common connection of the load.

CAUTION

Do not operate the DAP Digital Decoder Programmer with the remote sense input disconnected. Failure to observe this caution will result in the output of the power source exceeding the command by approximately 10%. This may result in damage to the system instruments and to equipment connected to the power source output.

3. Insert the power cord plug-in into a receptacle which provides the operating voltage specified on the rear nameplate of the DAP.

2.5 IEEE-488 Interface Connections

A DAP Digital Decoder Programmer equipped with the IEEE-488 interface option has a 24 pin connector, designated J103, mounted on the rear panel, which conforms to the requirements of IEEE specification 488-1975. Figure 2.3 shows the location of the terminals on this connector and Table 2.1 lists the signals which will be applied to each terminal. The common ground connection of J103 is connected to the ground return of the internal logic of the DAP and is isolated from the signal outputs, sense input and primary source ground connections.

When the electrical connections have been completed, perform the preoperational checkout of Section III. Successful completion of the preoperational checkout completes the installation.

2.6 BCD Input Connections

A DAP Digital Decoder Programmer internally connected for the 16 line BCD data input has a 37 pin connector, designated J103, mounted on the rear panel of the unit. A mating connector is provided. The signal lines which connect to each of the terminals of J103 are listed in Table 2.2. The common ground connection of J103 connects the ground return of the internal logic of the DAP and is isolated from the output signal, sense input signal, and primary power grounds. When the electrical connections are completed, perform the functional checkout of Section III. The successful completion of the functional checkout completes the installation.

NOTE

The DAP common is connected to the controller (computer) logic common and is normally grounded at the controller. If the controller interconnect cable is not connected to the DAP, the DAP common is floating.

TABLE 2.1. IEEE-488 INTERFACE INPUT CONNECTIONS

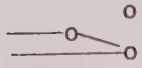
Connector J103
Programming Bus Connector 57-20240 Mating Connector 57-10240

Contact	Signal Line
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	Shield
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN
18	Gnd (6)
19	Gnd (7)
20	Gnd (8)
21	Gnd (9)
22	Gnd (10)
23	Gnd (11)
24	Logic Com.

Note: Gnd (n) refers to the signal com. return of the referenced contact.

TABLE 2.2. 16 LINE, BCD INPUT CONNECTIONS

J103: Programming Connector Cinch DC37P
Mating Connector Cinch DC37S Hood and Cable Clamp

		Amplitude Weight in Volts	Frequency Weight in Hertz	BØ & CØ Angle Weight in Degrees
1.	Logic Comm.			
2.				
3.	AØ Address			
4.	CØ Address			
5.	BØ Angle Address			
6.				
7.				
8.				
9.				
10.				
11.	Logic 2	.1V	X.1 Range	
12.	Logic 8	.1V		
13.	Logic 2	1V	1 Hz	1^{o}
14.	Logic 8	1V	1 Hz	1^{o}
15.	Logic 2	10V	10 Hz	10^{o}
16.	Logic 8	10V	10 Hz	10^{o}
17.	Logic 2	100V	100 Hz	100^{o}
18.	Logic 8		100 Hz	
19.				
20.	Logic Comm.			
21.				
22.	BØ Address			
23.	Frequency Address			
24.	CØ Angle Address			
25.				
26.	Isolated Contact Closure for	o Remote		
27.	Local Control Indication	 o Local		
28.				
29.	Logic 1	.1V	X1 Range	
30.	Logic 4	.1V		
31.	Logic 1	1V	1 Hz	1^{o}
32.	Logic 4	1V	1 Hz	1^{o}
33.	Logic 1	10V	10 Hz	10^{o}
34.	Logic 4	10V	10 Hz	10^{o}
35.	Logic 1	100V	100 Hz	100^{o}
36.	Logic 4	260 V Range (dual range option only)	100 Hz	
37.				

J101: Cinch DA-15S

Mating Connector Cinch DA-15P Signal Connector between DAP and Power Amplifier.

Cable supplied by Elgar Corporation between DAP and Power Amplifier(s) will be 2 feet unless otherwise specified.

Pin No.	Function
1	Common
2	B Signal
3	C Signal
4	A Signal
5	Spare
6	Spare
7	Spare
8	Spare
9	Spare
10	Spare
11	Spare
12	Spare
13	Spare
14	Spare
15	Spare

J102: Cinch DA-15P

Mating Connector Cinch DA-15S Remote Sensing (Amplitude Servos)

Pin No.	Function
1	Neutral
2	AØ Signal
3	BØ Signal
4	CØ Signal
5	Spare
6	Spare
7	Spare
8	Spare
9	Neutral
10	Spare
11	Spare
12	Spare
13	Spare
14	Spare
15	Spare

Figure 2.2 Sense & Signal Input Connector Data

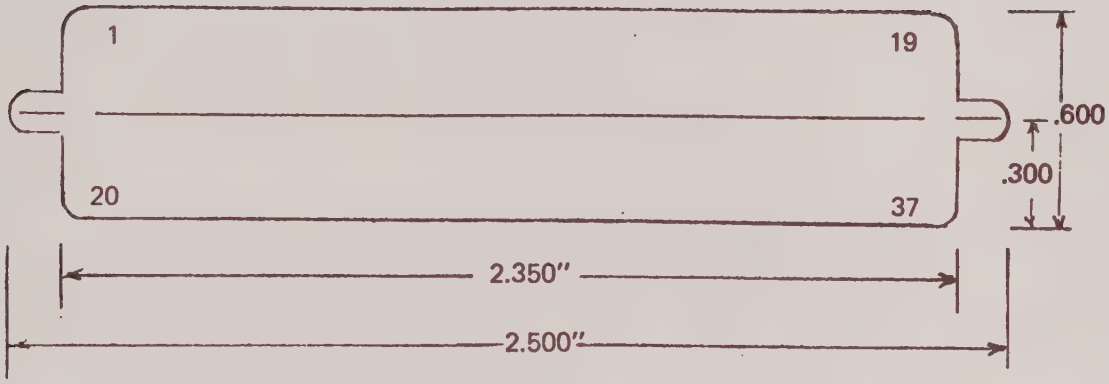


Figure 2.3. 16 Line, BCD Input Connector Dimensions

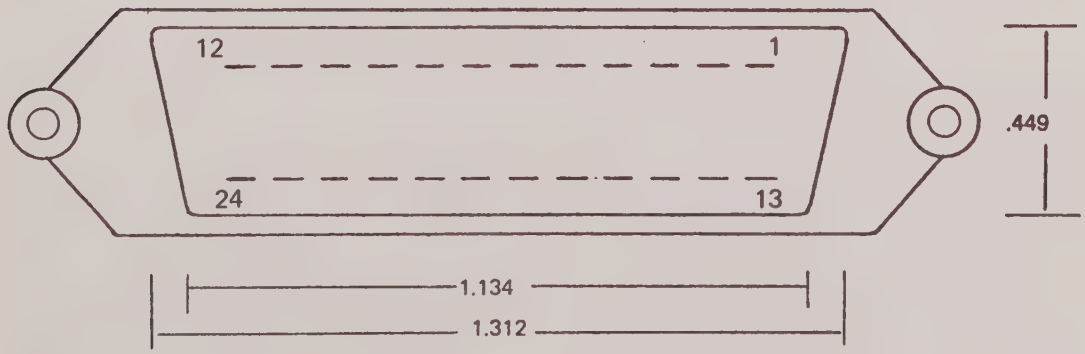


Figure 2.3. IEEE-488 Input Connector Dimensions

SECTION III
OPERATION

3.1 INTRODUCTION

This section contains information regarding the preliminary functional checkout of the Series DAP Digital Decoder Programmer as well as a description of front panel controls and indicators, rear panel outputs and inputs and complete remote programming information.

3.2 Controls and Indicators

The front panel controls and indicators of the DAP Digital Decoder Programmer are shown in Figure 3.1. Each of the front panel controls and indicators are described in the following paragraphs.

1. POWER ON-OFF SWITCH — Connects the primary power input to the power supply of the DAP.

2. POWER ON INDICATORS — This red indicator lights whenever power has been applied to the DAP.

3. REMOTE/LOCAL SWITCH — This switch will be installed only on units equipped with Option 1 or Option 2 (BCD Input) and that are also equipped with Option 5 (Front Panel Local Control). Units equipped with the IEEE-488 interface (Option -333) will not have this switch installed although Option 5 is installed. In that case, local control is obtained through a command from the system controller. When this switch is in the LOCAL position, control of the DAP, and the associated AC Power Source, is exercised through front panel switches. When the switch is in the LOCAL mode, the system controller cannot gain control of the DAP. Placing the switch in the REMOTE position permits the controller to program the outputs of the DAP.

4. FREQUENCY SWITCHES — This set of three or four pushbutton rotary switches enables the local operator to control the output frequency from 10 to 9990 Hz in the 3-range option, or 10 to 999 in the 1-range option. The one range option has 1 Hz resolution. In the three range option, the frequency may be adjusted in 0.1 Hz steps from 10 to 99.9 Hz, in 1 Hz steps from 100 Hz to 999 Hz and in 10 Hz steps from 1000 Hz to 9990 Hz. The multiplier switch allows the three preceding digits to be multiplied by 1/10, 1 or 10.

5. B-PHASE ANGLE SWITCHES — This set of three pushbutton rotary switches enables the local operator to adjust the BØ output phase angle in 1^{o} steps from 0^{o} to 359^{o} relative to the reference AØ.

6. C-PHASE ANGLE SWITCHES — This set of three pushbutton rotary switches enables the local operator to adjust the CØ output phase angle in 1^{o} steps from 0^{o} to 359^{o} relative to the reference AØ.

7. AMPLITUDE SWITCHES — This group of four pushbutton rotary switches enables

Figure 3.1. Front Panel Controls and Indicators

the local operator to adjust the output voltage of the associated power source in 0.1 volt steps from 0.05 volts to the maximum allowable output of the AC Power Source. The DAP that is equipped for two or three-phase operation, but without Option 8 (Independent Amplitude Programming) will have only one set of these amplitude programming switches which will control the output of all phases. With Option 8 installed, each phase will have its own set of amplitude programming switches which may be independently positioned.

CAUTION

The amplitude programming switches are not interlocked. Therefore, extreme caution should be exercised in setting these switches so that the maximum allowable output voltage of the AC Power Source is not exceeded. Failure to observe this caution may result in damage to the system instruments and to the load equipment.

8. FREQUENCY COMMAND DISPLAY – This red LED, 3 or 4-digit display reads the frequency command from the panel switches, when in local control and from the remote controller when operating in the remote mode. A movable decimal point allows the readout to display frequencies from 10 to 9990 Hz on the three range version.

9. B-PHASE ANGLE COMMAND DISPLAY – This red LED, 3-digit display reads the BØ angle command input from the panel switches when operating in the local mode and from the remote controller when operating in the remote mode.

10. C-PHASE ANGLE COMMAND DISPLAY – This red LED, 3-digit display reads the CØ angle command input from the panel switches when operating in the local mode and from the remote controller when operating in the remote mode.

11. AMPLITUDE COMMAND DISPLAY – When simultaneous amplitude programming is utilized, a single four digit, red LED display reads the amplitude command input from the front panel switches when in the local mode and from the remote controller when operating in the remote mode. When Option 8, Independent Amplitude Programming is installed, identical displays are installed for each phase with which the DAP is configured.

12. LISTEN INDICATOR – This green LED indicator is installed in those units in which Option -333, IEEE-488 Interface, is installed. It will be illuminated whenever the IEEE-488 Interface is in the listen mode.

13. REMOTE INDICATOR – This green LED indicator will be installed in those units in which Option -333, IEEE-488 Interface, is installed. It will be illuminated whenever the IEEE-488 Interface is operating in the remote mode.

3.3 Rear Panel Inputs/Outputs

There are three connectors on the rear panel of the DAP. One provides for the interconnection between the DAP and the remote controller, one provides for connection of the signal outputs from the DAP to the input of the associated power source and one provides for connection between the source output, or load, and the sense inputs of the DAP. The pin assignments of these connectors are covered in Section II.

3.4 IEEE-488 Programming

The Institute of Electrical and Electronic Engineers (IEEE) Standard 488-1975 specifies the method in which a central computer (controller) and the other devices in an automatic test equipment (ATE) system will communicate with each other. The DAP IEEE-488 interface option implements the following subsets of the IEEE-488 interface functions.

SH Function – SHØ
AH Function – AH1
T Function – TØ

L Function – L2
SR Function – SRØ
RL Function – RL2
PP Function – PPØ
DC Function – DCØ
DT Function – DTØ
C Function – CØ

This defines the interface as a listen only device with remote and local control capability, but without local lockout capability.

3.4.1 LISTEN Address

The "LISTEN" address, to which the DAP will respond, is determined by the positions of the individual switches of the 5-gang, DIP switch mounted on the IEEE-488 interface circuit board. Switches 1 through 5 of the gang switch correspond to bit 1 through bit 5, respectively, of the address message. The OFF position of each switch corresponds to the true state of the corresponding address bit. To set the discrete address, remove the top cover of the DAP and withdraw the IEEE interface board from its connector. (See Figure 7.2 for location of board.) The switch is located in the lower right corner of the circuit board. The digits 1 through 5, printed on the switch, identify the address bits 1 through 5. The combinations to which the switches are set will correspond to ASCII characters as shown in Table 3.1. To place a switch in its "ON" position, move it in the direction of the arrow. Moving it opposite the arrow will place it in the "OFF" position.

Setting of the address switches is the only adjustment required to place the DAP in operation except for the servo adjustments described in other paragraphs. When the address has been set with the switch assembly, replace the IEEE interface circuit board and the cover of the DAP.

3.4.2 Data Input Programming

A command message to the DAP consists of a string of ASCII characters for four decimal digits having values 0 through 9 followed by one of seven CAPITAL alphabetical characters, A through G. The most significant digit in the command is sent first followed by the next most significant, etc. The alphabetic character in the command identifies the function being programmed as follows:

A – A-Phase Voltage Amplitude
B – B-Phase Voltage Amplitude
C – C-Phase Voltage Amplitude
D – B-Phase Phase Angle
E – Simultaneous command for all phase amplitudes
F – Frequency, including range
G – C-Phase Phase Angle

The following six ASCII characters are forbidden in messages to the DAP since they represent numerical weights in excess of 9:

:
;
<
=
>
?

For the convenience of the programmer, non-message ASCII characters, other than those forbidden, may be interspersed in the message. These characters will be received, but not acted upon. The response time of the interface from the receipt of DAV true to the generation of NDAC false, is approximately 200 nanoseconds. The interface has storage capability for four decimal digits and, on receipt of a function identifier (alphabetical character), it commands the designated function with the last four digits received. It is, therefore, necessary that four digits be included in each command although, in some instances, they will have no significance. Storage registers, not part of the IEEE interface, are installed for each programmable function of the DAP. The commands are transferred to these storage registers which retain the last command received until a new command is received. When a function command is to be changed, it is only necessary to transmit the command for that function (or those functions to be changed). Commands may be sent in any order although the AC Power Source load requirements may dictate the order in which commands will be transmitted.

When power is applied to the DAP (Power ON), the storage registers external to the IEEE interface

TABLE 3.1. IEEE INTERFACE LISTEN ADDRESS

ASCII CHARACTER	IEEE Interface Board Settings				
	SW5	SW4	SW3	SW2	SW1
Space	ON	ON	ON	ON	ON
!	ON	ON	ON	ON	OFF
"	ON	ON	ON	OFF	ON
#	ON	ON	ON	OFF	OFF
$	ON	ON	OFF	ON	ON
%	ON	ON	OFF	ON	OFF
&	ON	ON	OFF	OFF	ON
'	ON	ON	OFF	OFF	OFF
(	ON	OFF	ON	ON	ON
)	ON	OFF	ON	ON	OFF
*	ON	OFF	ON	OFF	ON
+	ON	OFF	ON	OFF	OFF
,	ON	OFF	OFF	ON	ON
-	ON	OFF	OFF	ON	OFF
.	ON	OFF	OFF	OFF	ON
/	ON	OFF	OFF	OFF	OFF
0	OFF	ON	ON	ON	ON
1	OFF	ON	ON	ON	OFF
2	OFF	ON	ON	OFF	ON
3	OFF	ON	ON	OFF	OFF
4	OFF	ON	OFF	ON	ON
5	OFF	ON	OFF	ON	OFF
6	OFF	ON	OFF	OFF	ON
7	OFF	ON	OFF	OFF	OFF
8	OFF	OFF	ON	ON	ON
9	OFF	OFF	ON	ON	OFF
:	OFF	OFF	ON	OFF	ON
;	OFF	OFF	ON	OFF	OFF
<	OFF	OFF	OFF	ON	ON
=	OFF	OFF	OFF	ON	OFF
>	OFF	OFF	OFF	OFF	ON

assume a zero command if local control switches (Option 5) are not installed. If Option 5 is installed, the storage registers will assume the setting of the local control switches.

The most significant digit in the voltage command represents 100's of volts and the least significant represents 100's of millivolts. The most significant digit in the phase angle command represents 100's of degrees. The least significant is not acted upon as it would represent tenths of degrees whereas the angle resolution is limited to one degree. However, the fourth (least significant) digit must be transmitted to satisfy the message length requirements.

The most significant digit in the frequency command represents 100's of Hertz. In the single range frequency option, the least significant digit is not acted upon since it represents 0.1 Hz and the frequency resolution is limited to 1 Hz. However, the fourth (least significant) digit must be transmitted to satisfy the message length requirements. In the three range frequency option, the least significant is a range multiplier with the following values:

0 – X 10
1 – X 1
2 – X 1/10

This range digit must always be transmitted to satisfy the message length requirements. Also, in commands wherein the most significant digits are zeros, they must be transmitted to satisfy the message length requirements. For example, a command of 5.0V for phase A must be transmitted as 0050A. Multiple commands, that will command phase voltages, phase angles and frequency, may be transmitted without interspersing of spaces between individual commands. An example is given below:

A-Phase voltage	– 123.4V
B-Phase voltage	– 104.7V
C-Phase voltage	– 121.9V
Frequency	– 427 Hz

The above commands would, typically, be transmitted as follows:

1234A1047B1219C4271F

For the convenience of the programmer, additional characters having mnemonic significance may be inserted as follows:

123.4A 104.7B 121.9C 427R1F

These additional characters will not generate a strobe to load the registers in the IEEE-488 interface nor to transfer the contents of the registers into the function storage. Therefore, they will not interfere with the transmission of data to the DAP.

Each of the programmable functions of the DAP require 5 serial bytes of 7-bit parallel data which is satisfied by IEEE-488 input. The format is shown in Table 3.2. Input lines DIO1 through DIO4 carry the command data information with bit 4 being the most significant figure and bit 1 the least significant. Input lines DIO5, DIO6 and DIO7 provide steering information. When DIO5 and DIO6 are false, and DIO7 is true, the data on input lines DIO1 through DIO4 will be loaded into shift registers on the IEEE interface board.

When the data from bytes 1 through 4 have been loaded into the shift registers on the IEEE-488 interface circuit board, it must be loaded, during byte 5, into the storage registers of the appropriate logic board. The status of input lines DIO1 through DIO4 during byte 5 will determine which of the logic board receives the data stored in the IEEE-488 interface registers. Note that the state of input lines DIO5 through DIO7 are reversed in byte 5 from what they were in bytes 1 through 4. These three bits provide steering information for the data on input lines DIO1 through DIO4. Note that if the amplitude of all three output phases are to be identical, that the data in the IEEE-488 interface registers may be simultaneously loaded into the storage registers of all three amplitude logic boards, by the proper coding of input lines DIO1 through DIO7. Frequency, angle and amplitude data may be loaded in any sequence required by the program and it is only necessary to transmit that data which constitutes a change in one of the functions of the DAP. In most cases, the amplitude of all three phases will be programmed to zero before changing frequency or phase angle.

Note that phase angle and single range frequency

TABLE 3.2. IEEE-488 DEVICE DEPENDENT INPUT DATA FORMAT

Input Line	Most Significant Digit Byte 1	Byte 2	Byte 3	Least Significant Digit Byte 4	Byte 5 (See Text) Frequency	BØ Angle	CØ Angle	AØ Amplitude	BØ Amplitude	CØ Amplitude	AØ, BØ, CØ Amplitude
DIO1	100	10	1	.1	F	F	T	T	F	T	T
DIO2	200	20	2	.2	T	F	T	F	T	T	F
DIO3	400*	40	4	.4	T	T	T	F	F	F	T
DIO4	800	80	8	.8	F	F	F	F	F	F	F
DIO5	T	T	T	T	F	F	F	F	F	F	F
DIO6	T	T	T	T	F	F	F	F	F	F	F
DIO7	F	F	F	F	T	T	T	T	T	T	T
DIO8	X	X	X	X	X	X	X	X	X	X	X

800, 80, 8 etc. = TRUE

T = TRUE
F = FALSE
X = IRRELEVANT

*Note: This bit must be true to program 260V range on units configured for 130V/260V.

inputs require only the information contained in bytes 1, 2 and 3. However, byte 4 must be transmitted so that the first three bytes of information will be clocked through to the proper position in the shift registers of the IEEE- 488 interface circuit board. The actual states of inputs lines DIO1 through DIO4 in byte 4 are, in these instances, of no consequence.

3.5 BCD Input Programming

The BCD input connector, J103, on the rear panel of the DAP has terminals for 16 lines of data input, 6 for logic circuit board address, and one to command voltage range. The assignments of each terminal of this connector as shown in Section II, Table 2.2. The input lines are coded in BCD then the appropriate address line is held true to load the input data into the storage register of the logic circuit board. When the address lines goes false, the data will remain in storage on the logic board and the data input lines may then be recoded with data for direction to another logic board. The sequence in which data may be addressed to the various logic boards will be at the option of the programmer. Generally, however, all data input lines will be set to zero and all three amplitude address lines held low to set the output of the DAP at zero. Frequency and phase angles will then be programmed and then the AØ, BØ, and CØ amplitudes will be programmed. Note that with Option 8 each phase amplitude output may be programmed individually, if they are to be at different levels, or they may be programmed simultaneously if they are to be at the same level. To program them simultaneously, the data lines for the amplitude logic boards held true simultaneously.

3.6 Logic Operation (Parallel BCD Inputs)

Units equipped with Option 1 or Option 2 (Parallel BCD Inputs) will have REMOTE/LOCAL switch on the front panel if Option 5 (Local Control) is installed. The switch will normally be in the REMOTE position enabling the remote controller to introduce commands into the unit through the rear panel connector.

To transfer control to the front panel switches, the REMOTE/LOCAL switch is placed in the LOCAL position. The remote controller will then be unable to take command of the DAP. When the REMOTE/LOCAL switch is placed in the LOCAL position, the DAP will immediately generate outputs which have frequency, phase angles and amplitudes that are set into the front panel switches. Therefore, caution should be exercised when making the transfer from remote to local operation that the front panel switch positions are compatible with the load connected to the output of the power source.

When the REMOTE/LOCAL switch is returned to the REMOTE position, the panel switches will be disconnected, however, if storage logic (Option 3) is installed, the data set in the panel switches at the time of the local-to-remote transfer will control each output of the DAP until the system controller transmits new data for each of the DAP functions. This occurs because the local-to-remote transfer stores the front panel switch data on the logic board outputs.

This temporary retention of panel data may be used to advantage when inputs to the power source are to be generated only in response to front panel switch settings. If the rear panel control input is disconnected, or the controller is otherwise prevented from inputting data into the DAP, data may be entered with the panel switches while the REMOTE/LOCAL switch is in the LOCAL position. Returning it to the remote position will store that data. The panel switches may then be set with new data. When the switch is returned to the LOCAL position the new data will immediately control the power source. Returning the switch to REMOTE then stores that data while new data is again set into the switches. This sequence is repeated as often as necessary.

Units equipped with the IEEE-488 interface do not have a REMOTE/LOCAL switch on the front panel. These units will power up in the local mode. If they are operating in the remote mode, the remote controller must command the unit to the local mode or the DAP must be turned off and then back on at which time it will be in the local mode until commanded into the remote mode by the remote controller.

3.6.1 Amplitude Programming

Option 5 provides amplitude programming from front panel mounted pushbutton rotary switches. A single set of four switches will control the amplitude of all phases unless Option 8, Independent Amplitude Programming, is installed. With Option 8 installed, each phase has its own set of four pushbutton rotary switches for amplitude programming. The switches enable the operator to adjust the amplitude of the AC Power Source output from 0.5 V to the maximum output for which the AC Power Source was designed. The switch for the most significant digit is limited in travel from 0 to 1 for those units of the DAP configured with the 150V Servo circuit boards. On those with Option 7 the 130V/260V Servo circuit boards, the switch for the most significant digit is limited in travel from 0 to 2. The other switches are not interlocked therefore, care should be exercised in the operation of the switches so that the amplitude command is not greater than that for which the associated power source is designed. Also, it is possible to set the output voltage of each leg at a different level. In some systems this may be desirable and necessary, however, care must be exercised that the amplitude settings are compatible with the load connected to the power source.

On those units of the DAP equipped with the 130V/260V Servo circuit boards, the RANGE switch on the front panel must be set to the 260V position whenever the setting of the switches is greater than 130V. Also, it should be set to the 130V position whenever the amplitude setting of the switch is for 130V or less. In addition to setting the gain of the output amplifiers on the circuit boards, commensurate with the selected output voltage, the RANGE switch may also operate relays in the power source that will connect the secondary windings of the power source transformers either in series or parallel, depending on the selected range, so that full power may be generated at the selected voltage.

3.6.2 Phase Angle Programming

The AØ signal from the DAP is the reference phase, therefore, pushbutton rotary switches are provided only for the B-phase in a 2-phase system and for the B-phase and C-phase in a 3-phase system. Each programmable phase has a set of three switches which permit the operator to adjust the phase angle, relative to the reference phase, from 1^{o} to 359^{o}. It is possible to command phase angles in excess of 360^{o} and the DAP will respond to that type of input. However, a 360^{o} setting would place that phase in-phase with the reference phase. A 390^{o} setting would result in the signal leading the reference by 30^{o}.

3.6.3 Frequency Programming

When operating in the local mode, the internal programmable oscillator is controlled by three or four pushbutton rotary switches on the front panel which permit the operator to adjust the frequency from 10 Hz to 999 Hz in 1 range or 10 Hz to 9990 Hz in three ranges, depending on the frequency option selected. The first switch selects the most significant digit, the second selects the next most significant digit and the third selects the least significant digit. The fourth switch is a range selector and is labeled X1/10, X1, and X10. The setting of the first three switches will be multiplied by a factor indicated by the setting of the fourth. When the range selector switch is in the X1/10 position, the frequency is adjustable in 0.1 Hz steps. When it is in the X1 position, the frequency is adjusted in 1 Hz steps. When it is in the X10 position, the frequency is adjustable in 10 Hz steps.

CAUTION

Although the DAP, with frequency programming, has the capability of generating frequencies as low as 10 Hz, most Elgar AC Power Sources have a low frequency limit of 45 Hz. Therefore, the DAP should not be programmed for frequencies below 45 Hz unless the associated AC Power Source is known to be designed for lower frequencies.

3.7 Functional Checkout

The functional checkout verifies that the Digital Decoder Programmer is functioning normally. The functional checkout does not verify accuracy, response time or resolution. For specification validation, refer to checkout procedures in Section V. The functional checkout should be per-

formed with the Digital Decoder Programmer installed in the system and properly connected to the program source, associated AC Power Source and facility line power. (Refer to Section II for proper installation procedures.) The functional checkout assumes that the unit under test is equipped with a complete set of options. Those tests that require the operation of functions not included in the unit under test should be ignored. The functional checkout includes operation of all front panel controls and indicators and a check of the remote input program response.

3.7.1 Preliminary Set-Up

Before starting the functional check, verify the following:

1. DAP power switch at off.
2. AC Power Source switch at off.
3. Program Source (computer, tape deck, etc.) de-energized or in standby condition.
4. Any load is disconnected from the AC Power Source.
5. Remote sense leads connected to output of AC Power Source.

3.7.2 Local Mode Check

The following procedure assumes a fully configured DAP with frequency, phase angle and amplitude programming. If the unit is equipped with input command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit steps for those functions not included in the DAP under test.

Proceed as follows to check operation of the DAP in the LOCAL MODE:

1. If the unit has -1 or -2 BCD programming, place the REMOTE/LOCAL switch in the LOCAL position. With the -333 option, the unit will remain in local control until commanded remotely into remote control.
2. Set all AMPLITUDE SWITCHES to zero.
3. Connect a frequency meter and a digital voltmeter between the HI-LO front panel test posts of the AC Power Source.
4. Connect phase meters between the AØ output and the BØ and CØ outputs of the AC Power Source.
5. Set the FREQUENCY switches to 450 X1/10 for 3 range option or 045 for 1 range option.
6. If the DAP is equipped with a front panel Range Switch, place it in the 130V position.
7. Set the associated AC Power Source Power Switch to ON (refer to AC Power Source instruction manual for AC Power Source operating procedure).
8. Place the DAP Power Switch to ON and verify that the power indicator lights.
9. Verify that the AC Power Source voltmeter reads 0 volts.
10. Set the BØ ANGLE switches to 240^{o} and the CØ ANGLE switches to 120^{o}.
11. Set the AMPLITUDE switches to 000.5.
12. Verify that the AC Power Source voltmeter reads 0.5 volts and verify that the frequency is 45 Hz.
13. Increase the output of all phases of the AC Power Source with the AMPLITUDE switches in 0.1 volt steps from 0.5 to 1.5V.
14. Verify that the AC Power Source voltmeter indicates corresponding increases in output voltage.
15. Set all three groups of AMPLITUDE switches on the DAP to 010.0.
16. Increase the output of all three phases of

the AC Power Source with the AMPLITUDE switches from 10.0 volts to 19.0 volts in 1.0 volt steps. Verify that the AC Power Source increases by 1.0 volts with each switch position change.

17. Increase the output of all three phases of the AC Power Source with the AMPLITUDE switches from 19.0 volts to 130.0 volts in 10.0 volt steps. Verify that the AC Power Source output increases by 10 volts with each switch position change.

18. If the DAP is equipped with a 260 volt servo board or 130V/260V servo board, increase the output of all three phases of the AC Power Source to 260 volts in 10 volt steps. (If equipped with 130V/260V servo, place 130V/260V switch in 260V position.) Verify an increase in AC Power Source output of 10 volts with each switch position change.

19. For the three range frequency option, set the FREQUENCY range switch to the X1 position and verify that the output frequency of the AC Power Source increases to 450 Hz and that the BØ and CØ remain at 120^{o} and 240^{o}. For the single range frequency option, increase the frequency in 100 Hz steps to 950 Hz and verify that the output frequency of the AC Power Source increases to 950 Hz.

20. For the three range frequency option, set the FREQUENCY range switch to the X10 position and verify that the AC Power Source output frequency increases to 4500 Hz and that the BØ and CØ angles remain at 240^{o} and 120^{o}.

21. Reset the FREQUENCY to 45 Hz and verify frequency and that the BØ and CØ angles remain at 120^{o} and 240^{o}.

Note: The following steps, 22 to 25, are primarily for the 3 range frequency option.

22. Increase the frequency from 45 Hz to 45.9 Hz in 0.1 Hz steps and verify that the output frequency of the AC Power Source increases accordingly.

23. Increase the frequency from 50 to 90 Hz in 10 Hz steps and verify that the output of the AC Power Source increases accordingly.

24. Return the FREQUENCY switches to 100 and set the FREQUENCY range switch to X10 and verify that the output frequency of the AC Power Source is now 1000 Hz.

25. Increase the frequency from 1000 Hz to 9900 Hz in 100 Hz steps and verify that the output of the AC Power Source changes accordingly. Reset frequency to 400 Hz.

26. Set the BØ ANGLE switches to 000. Increase the BØ angle from 0^{o} to 10^{o} in 1^{o} steps and verify that the BØ output of the AC Power Source changes in accordance with the switch changes.

27. Increase the BØ angle from 10^{o} to 350^{o} in 10^{o} steps and verify that BØ output of the AC Power Source changes in accordance with the switch changes.

28. Repeat steps 26 and 27 for the CØ output.

29. Set the AMPLITUDE switches on the DAP to 000.0. Turn the Power switch on the AC Power Source to OFF. Turn the Power switch on the DAP to OFF.

If any malfunction of the DAP, or the AC Power Source, is determined during the local mode check, the problem should be corrected before performing the remote check.

3.7.3 Remote Mode Check (IEEE-488)

For those programmers with the GPIB IEEE 488 interface (Option -333) there is NO LOCAL/REMOTE switch. At turn on the programmer outputs will go to the command levels of the local control switches. The local commands will remain in storage until the handshake sequence is completed, REN is true, and a function receives a 5 byte command.

The remote mode checkout consists of programming the digital decoder programmer input for a voltage sweep throughout the range of 0 to 130V (or 130V/260V as appropriate) and checking the frequency stability at low, intermediate, and high frequency ranges. If a test program is available in the controller, the AC Power Source outputs can be recorded and the test may be accomplished automatically. If a test program is not available, some means of simulating the programming in accordance with IEEE Standard 488-1975, including the device dependent programming defined in the section, must be devised and entered through the rear panel connector, J103.

The following procedure assumes a fully configured DAP with frequency, phase angle and amplitude programming. If the unit is equipped with input command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit those steps or those functions not included in the DAP under test.

1. Verify that the Power switches on both the AC Power Source and DAP are in the OFF position.

2. Connect the program source to the rear panel connector, J103, on the DAP.

3. Connect a frequency meter to the output test posts on the front panel of the AC Power Source. Also, if the DAP is configured for phase angle programming, connect frequency meters between the AØ and BØ and the AØ and CØ outputs of the AC Power Source.

4. Turn the Power switch on the AC Power Source to ON.

5. Place the Power switch on the DAP to ON. Verify that the POWER indicator is illuminated and that the LISTEN and REMOTE indicators are extinguished.

6. Disable the remote function of the program source and program the address for the DAP. Verify that the LISTEN indicator on the DAP is illuminated and that the REMOTE indicator remains extinguished.

7. Program the "unlisten" command and verify that the LISTEN indicator on the DAP panel is extinguished.

8. Enable the remote function of the program source and program the address of the DAP. Verify that the LISTEN and REMOTE indicators are both illuminated.

9. Program 50 Hz.

10. Program the BØ angle at 120^{o}.

11. Program the CØ angle at 240^{o}.

12. Simultaneously, program all three phase amplitudes to 100V. Verify that the AC Power Source output is 100V, that the frequency is 50 Hz and that the BØ and CØ angles are 120^{o} and 240^{o} respectively.

13. Simultaneously, program all three amplitudes to 0.5V. Verify that the AC Power Source output is 0.5V and that frequency is 50 Hz.

14. Program 1.5V and verify that the AC Power Source output is 1.5V.

15. Program the system to 2.5V in 0.1V steps. Verify that the output of the AC Power Source follows the program steps.

16. Program the system from 1 to 10 volts in 1 volt steps. Verify that the output of the AC Power Source follows each program step and that the frequency remains at 50 Hz.

17. Program the system to 130V in 10V steps and verify that the AC Power Source output follows each step of the program. Also, verify that the frequency remains at 50 Hz and that the phase angles remain at 120^{o} and 240^{o}.

18. If the DAP and the AC Power Source are designed for 130V/260V operation, program the system to 260V in 10V steps and verify that the AC Power Source follows each step of the program and that the frequency remains at 50 Hz and the phase angles remain at 120^{o} and 240^{o}.

19. Program all three phase amplitudes to 100V.

20. Program the AØ amplitude to 110V. Verify that the AØ of the AC Power Source is at 110V and the other 2 phases remain at 100V.

21. Program the BØ to 110V and verify that the BØ output of the AC Power Source is at 110V, that the AØ amplitude is 110V and the CØ output is 100V.

22. Program the CØ amplitude to 110V and verify that the CØ output of the AC Power Source is now 110V and that the AØ and BØ remain at 110V.

23. Program the frequency to 45 Hz. Verify that the frequency output of the AC Power Source is now 45 Hz.

24. Program the frequency from 45 Hz to 45.9 Hz in 0.1 Hz steps. Verify that the output frequency of the AC Power Source follows each step of the program.

25. Program the frequency from 50 Hz to 100 Hz in 10 Hz steps and verify that the frequency of the AC Power Source output follows each step of the program.

26. Program the frequency from 100 to 1000 Hz in 100 Hz steps and verify that the frequency output of the AC Power Source follows each step of the program.

27. Program the frequency from 1000 Hz to 9000 Hz in 1000 Hz steps and verify that the frequency output of the AC Power Source follows each step of the program.

28. Program the frequency from 9000 Hz to 9900 Hz in 100 Hz steps and verify that the frequency output of the AC Power Source follows each step of the program.

29. Program the frequency to 400 Hz.

30. Program the BØ signal from 0 to 10^{o} in 1^{o} steps. Verify that the BØ output of the AC Power Source follows each step of the program.

31. Program the BØ angle from 10^{o} to 100^{o} in 10^{o} steps and verify that the BØ output of the AC Power Source follows each step of the program.

32. Program the BØ phase angle from 100 to 300^{o} in 100^{o} steps and verify that the BØ output of the AC Power Source follows each step of the program.

33. Program the BØ angle from 300^{o} to 360^{o} in 10^{o} steps and verify that the BØ output of the AC Power Source follows each step of the program.

34. Repeat steps 30, 31, 32, and 33 for the CØ output.

35. Simultaneously, program all AMPLITUDE outputs to zero.

36. Program the GTL (GO TO LOCAL) command and verify that the REMOTE indicator on the DAP panel is extinguished.

37. Program the UNL (UNLISTEN) command and verify that the LISTEN indicator of the DAP panel is extinguished.

38. Turn the Power switch on the DAP OFF and the Power switch on the AC Power Source to OFF.

39. Disconnect the program source.

This concludes the operational check of the DAP.

3.8 Operating Instructions

In the remote mode, the DAP Digital Decoder Programmer is under command of the remote programming source (controller) and this is the normal mode of operation. The local control capability of the DAP is advantageous for some phases of the initial system checkout and for test purposes when troubleshooting system problems. In the local mode, the DAP is manually operated through front panel switches that control each function.

3.8.1 Remote Mode BCD Inputs

For programmers with BCD parallel logic level inputs (Options -1 or -2) the output of the programmer will go to the command levels present at J103 the logic connector. For those programmers with BCD parallel logic pulse inputs with internal storage (Option -1 or -2 with Option -3) the output of the programmer will go to the command levels of the local control switches and remain there until address strobes are received from the remote controller.

To place the decoder programmer in the remote mode of operation, proceed as follows:

1. Turn the Power switch on the AC Power Source to ON.

NOTE

The AC Power Source should always be turned on before the DAP. Otherwise, if the DAP is programmed for maximum output from the AC Power Source, it will, momentarily, drive the AC Power Source output to a level 10% or more above the command voltage. This may cause damage to the load or other system instruments.

2. Turn the Power switch on the DAP to ON and verify that the Power indicator is illuminated.

3. Set the REMOTE/LOCAL switch to the REMOTE position or command the remote mode as appropriate to the unit under test.

4. The DAP is now energized and enabled to receive programmed inputs from the controller. The recommended program sequence is as follows:

   A. Program amplitude to zero.
   B. Program frequency.
   C. Program phase angles.
   D. Program amplitudes.

NOTE

The DAP should not be programmed for frequencies below 45 Hz. To ignore this caution may cause damage to other system components.

3.8.2 Local Mode

To operate the decoder programmer in the local mode, proceed as follows:

1. Verify that the Power switches on the AC Power Source and the DAP are in the OFF position.

2. Set the DAP REMOTE/LOCAL switch to LOCAL or command the local mode as appropriate to the unit under test.

3. Set the FREQUENCY, PHASE ANGLE and AMPLITUDE control switches to the desired values.

4. Place the Power switch on the AC Power Source to ON.

5. Place the Power switch on the DAP to ON. Verify that the POWER indicator on the DAP is illuminated, and that the voltmeter on the AC Power Source coincides with the amplitude setting of the front panel amplitude control switches. If the DAP is equipped with command input displays, verify that the display indications coincide with the setting of the panel switches.

CAUTION

Do not attempt operation of the DAP Digital Decoder Programmer outside

of ranges specified in Table 1.2 or the specified ranges of the AC Power Source. Failure to observe this caution may result in damage to system instruments.

If the operational or test program will require a number of frequency, phase angle or amplitude changes, and the unit is equipped with Option 3 (Storage), it may be desirable to use a special feature of the DAP Digital Decoder Programmer. If the controller input is removed from J103, the DAP will retain the program data entered with the panel switches when the REMOTE/LOCAL switch is placed in the REMOTE position. While the system is operating with that data, new data may be set into the front panel switches. When the REMOTE/LOCAL switch is returned to the LOCAL position, the outputs of the DAP will take on the frequency, phase angles and amplitudes as set in the panel switches. By use of this feature, all programmed data may be entered simultaneously.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section contains an overall description of the operation of the DAP Digital Programmer as well as the description of each major circuit in the instrument for which this manual was prepared.

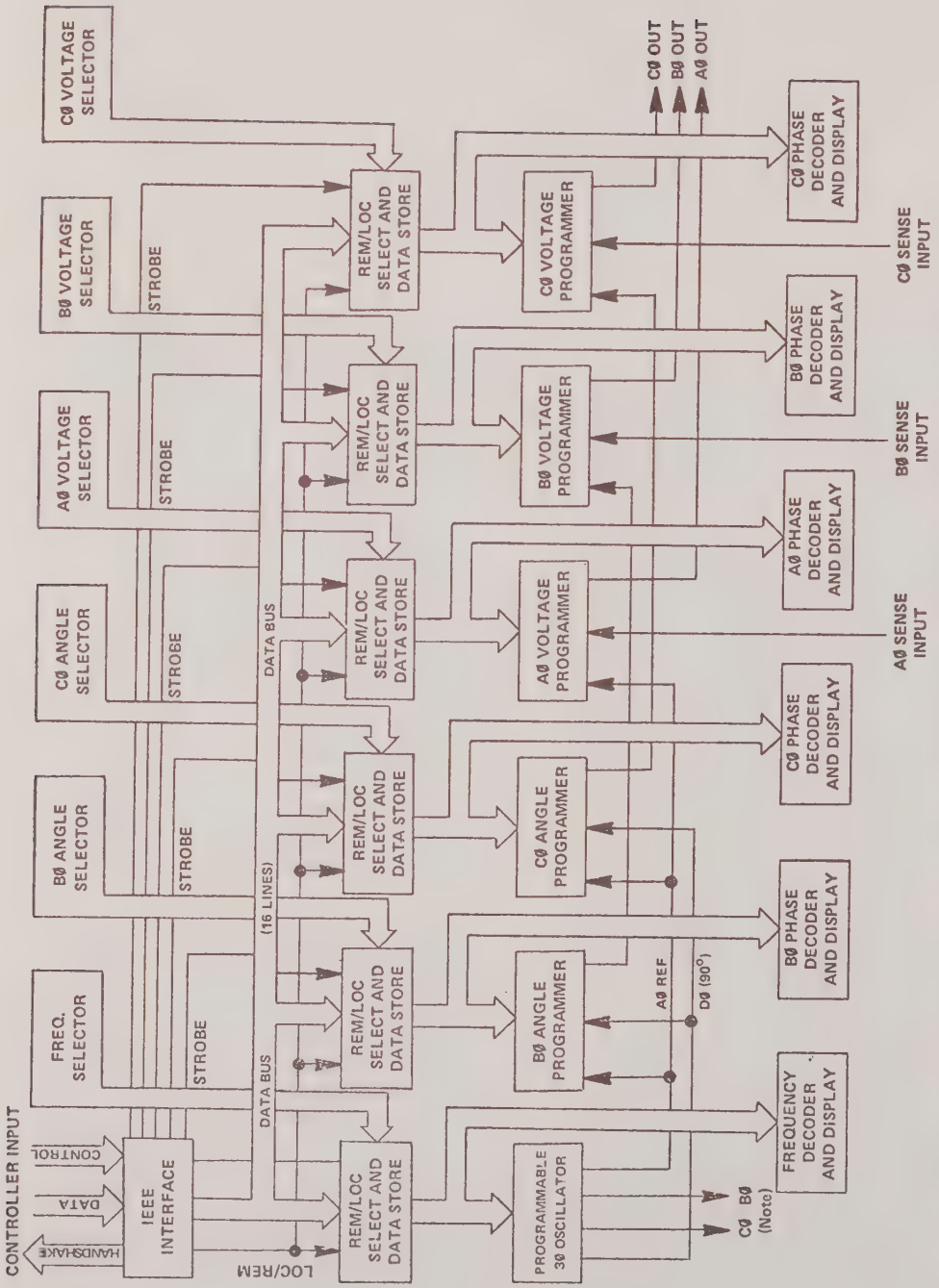
This section is organized to present a functional description of the DAP configured with the IEEE interface and programming capability for the oscillator, BØ angle programmer, CØ angle programmer, voltage programmers for all three phases, local controls for all functions and display of command data. Following this function description, detailed descriptions are provided for the mother board, power supply and each circuit board, function selector or display system included in the unit for which this manual was prepared.

In general, this section is intended to aid in understanding how the DAP functions and should be reviewed prior to troubleshooting or attempting to optimize DAP applications.

4.2 OVERALL THEORY OF OPERATION

A block diagram of the DAP is shown in Figure 4.2.1. The power sources for the circuits within the DAP are not shown. The REM/LOC Select and Data Store block in Figure 4.2.1 represent a plug-in circuit board. When power is first applied, these circuit boards are automatically placed in the local condition. If the local function controls are installed, the data supplied to the programmable oscillator, angle programmers and voltage programmers will be that data set into the front panel thumbwheel switches of the function controls. If the function controls are not installed, all data outputs will be 0. The IEEE interface provides a means of paralleling a number of devices on a single bus with all devices having uniform input connectors and connections. Of the six lines of the control bus, the DAP accepts information from only four. There are eight lines on the data bus and the DAP accepts information from seven. The handshake bus has two lines and they indicate to the controller when the DAP is able to accept data and when it has accepted data. For the DAP to respond to the controller commands, the controller must first send a discrete, seven-bit address code of which five bits are selectable within the DAP, along with the REMOTE ENABLE command and the proper control signals. The DAP will remain in the remote mode, as long as REMOTE ENABLE is true.

When the controller has transmitted the discrete address to the DAP, it will be acknowledged through the handshake bus and the DAP will then be in the listen mode and will be able to receive and respond to the controller's commands. Each function of the DAP requires sixteen bits of data. These are transmitted in four serial bytes of four parallel bits each. The IEEE interface board has temporary storage for the data bytes. The four bytes of data are followed by a "steering" byte that generates a strobe pulse to load the data, temporarily stored in the IEEE interface, into permanent storage on the selected REM/LOC Select and Data Storage board. The previously transmitted REMOTE ENABLE command will place all the data storage boards in a condition to



NOTE: These outputs from oscillator connected directly to voltage programmer when phase angle programmer is not installed.

Figure 4.2.1. Block Diagram, DAP Decoder Programmer

receive remote data from the IEEE interface. When the data is loaded into permanent storage, the programmer connected to the storage board will immediately respond to the command.

When the DAP is in the local mode, and provided that the local function controls are installed, the data bus from the function control is connected directly to the output of the REM/LOC Select and Data Storage board and a strobe pulse is not required to transfer this data to the output. The local function controls enable local selection of frequency, BØ angle, CØ angle, and the individual voltage level of all three phases. The output of the REM/LOC Select and Data Storage boards are also applied to decoder drivers that drive seven-segment LED displays.

The programmable oscillator develops 3Ø output and a 4th phase, identified as DØ that lags the AØ output by 90°. When phase angle programmers are installed in the DAP, the AØ and DØ are applied to the BØ angle and CØ angle programmers. Circuits within the programmers combine these two signals to produce an output phase to satisfy the input command. The AØ output of the oscillator and the outputs of the two phase angle programmers are individually applied to the voltage programmer for each phase. Each voltage programmer generates an output that is in phase with its input and which has a level corresponding to the input command. The outputs provide the input signal for the associated power source. The sense input signals are obtained from the secondaries of transformers connected across the load of each phase of the power source. These inputs are compared to the command input and correct the output of the voltage programmers so that the voltage across the load is maintained at the command voltage.

When phase angle programmers are not installed, the BØ and CØ outputs of the programmable oscillator are connected directly to the input of the BØ voltage programmer and the CØ voltage programmer. The 3Ø outputs will then have 120° phase separation.

The foregoing functional description is for a DAP that has all of the compatible options installed. A block diagram for the DAP for which this manual is prepared, would be somewhat simplified, for example, if the function selectors and displays are omitted and the BØ and CØ angles where not programmed. It is not practical to develop a block diagram for each DAP showing only the functions with which it is configured.

4.3 DETAILED CIRCUIT DESCRIPTION

In the following paragraphs, those circuits that are part of the particular DAP unit for which this manual was assembled are described in detail. In preparing the following text it has been assumed that the technician is familiar with analog and logic devices such as operational amplifiers, logic gates, adders, data selectors and digital-to-analog converters. Therefore, the internal circuitry of the integrated circuits that provide these functions are not described in detail. The technician is referred to manufacturer's publications and other available data for those descriptions.

Where an integrated circuit contains a number of identical devices, the individual devices will be identified with the integrated circuit number and a suffix letter or the individual output terminal number if a suffix letter is not assigned. For an example of the latter case, U302-7 identified an operational amplifier which is part of integrated circuit U302 that has its output connected to pin 7 of that device. In general, the descriptions of this subsection are referenced to the schematic diagrams which will be found in Section VII.

4.3.1 Interconnect (Mother Board)

The schematic diagram of the interconnect (mother) board is shown in Figure 7.1. The mother board is universal to all units of the DAP regardless of the number or types of circuit boards installed. The diagram of Figure 7.1 shows each connector which may be installed on the mother board. However, connectors will be installed only for those circuit boards that are required to provide the functions specified by the individual customer. Likewise, the front panel rotary push-button switches and seven-segment LED readout devices, although shown in Figure 7.1, will be

installed only if specified by the customer. The mother board has provisions for the installation of as many as 13 circuit boards. The functions of these 13 circuit boards are as follows:

1. IEEE Interface Board. Provides interface between a computer bus conforming to IEEE standard 488-1975 and the inputs to the various logic cards of the DAP.

2. Oscillator Logic. Selects remote or local inputs to be applied to the oscillator board. May or may not have internal storage capability.

3. Oscillator Board. The fixed oscillator board does not require the oscillator logic board and generally produces a 3Ø output at 400 Hz although other frequencies may be specified by the customer. The programmable oscillator accepts BCD input commands to vary the oscillator frequency from 10 Hz to 9990 Hz in three decade ranges. The programmable oscillator also produces 3Ø outputs.

4. Phase Logic Boards. One or two of the phase logic boards may be installed, one for each programmable phase angle. These are identical in circuitry to the oscillator logic board and may, or may not, have internal storage. Their primary purpose is to select between local and remote inputs for application to the programmable phase angle boards.

5. Phase Angle Boards. There are positions for two phase angle boards. These are for the BØ and CØ only as the AØ is the reference phase. In response to inputs from the respective logic boards, the phase angle boards may be programmed to produce output signals from 0^{o} to 359^{o} relative to the reference phase. If these boards are not installed, and the system is to be operated 3Ø with the BØ and CØ operating at + and $-$ 120^{o} from the reference phase, jumpers will be installed, between the phase output from the oscillator board and terminal 14 of the servo boards, Item 7.

6. Servo Logic Boards. When the unit is not equipped with Option 8 (Independent Amplitude Programming) a single servo logic board will be installed and jumper cables will connect its output to all servo boards installed in the unit. When Option 8 is installed, a logic board will be installed for each of the phases. The purpose of the logic board is to provide selection between local and remote control of the associated servo board(s). These logic boards are identical to the oscillator logic and phase logic boards. They may, or may not, have internal storage capability.

7. Servo Boards. A servo board will be installed for each of the active phases of a system. If the system is single phase, only one servo board will be installed. If the system is operating three phase, then three servo boards will be installed. The servo boards accept BCD input from the associated logic board and an input from a sense transformer which has its primary winding connected across the load of the associated power source. In response to a BCD input command, the servo board will drive the output of one phase of the associated power source to the voltage commanded by the BCD input. It will continually compare the BCD command signal to the input from the sense transformer to maintain the voltage across the load at the command voltage.

Note that there are two connectors, shown adjacent to the IEEE interface circuit board, they are labeled J103. J103 is the rear panel mounted, computer input connector. When the IEEE interface board is utilized, J103 is a 24 pin connector. When the sixteen line, BCD input and seven control lines are used, J103 is a 37 pin connector. Either connector will be connected to the mother board as shown in Figure 7.1.

Figure 7.1 shows local control pushbutton rotary switches for frequency, the three phase angles and the three phase amplitude controls.

This is a customer selection option (Option 5). If installed, local control may be selected with a front panel switch on those units configured with Option 1 or 2 (Parallel BCD Inputs). When the IEEE-488 interface is installed, local control is acquired at power on or, if the unit has been operating in the remote mode, by a command from the system controller. Figure 7.1 also shows digital readouts for frequency, BØ and CØ angles and the three phase amplitudes. These are installed as Option 6. Note that the decoder/drivers and their seven-segment LED readouts decode and display the command signal. If the local control pushbutton rotary switches and/or the digital readouts have been selected for installation in the DAP unit for which this manual was issued, the function of the circuits associated with these devices is covered in later paragraphs.

Note that the ground returns for the various DAP inputs are isolated one from another. The power transformer, and the sense and output transformers are all equipped with electrostatic shields which are grounded to the chassis. The output transformers share a common connection which is connected to the common connection at the input of the associated power source. The sense transformers also share a common connection which is connected to the common connection of the associated power source load. The ground return for the logic of the DAP is common with the ground return for the input of the associated controlling computer. Finally, the chassis of the DAP is grounded to the center pin of the power connector.

4.3.2 Storage Logic Board

The schematic diagram for the storage logic board is shown in Figure 7.6. The primary function of the storage logic board is to select between remote and local command inputs in response to computer or front panel inputs. The circuitry consists of 4 data selectors, U202, U203, U204 and U205, four quad D-latches and a triple, 3-input NAND gate. The data selectors connect the local command inputs to the output when terminal 1 is high and connect the remote inputs to the outputs when terminal 1 is low. Data is transferred from the input of the quad D-latches when terminals 4 and 13 are high. When the circuit board is under local control, terminals 4 and 13 of the quad D-latches are held high continuously since the panel switches provide the storage capability. Any change in the setting of the switches will be immediately transferred to the output of the quad D-latches. When operating in the remote mode, terminals 4 and 13 of the quad D-latches are normally held low. A strobe pulse, at terminal 15 of the circuit board connector, will clock terminals 4 and 13 of the quad D-latches to transfer the remote data to their outputs.

When power is first applied, the voltage at the junction of R201 and C202, which is applied to the inputs of U201-12 and U201-6, will be held low for approximately .02 seconds. This will set the latch, comprised of U201-6 and U201-8, with U201-6 high. This will cause the data selectors to select the local inputs. At the same time, the output of U201-12 will be high and the outputs of the selectors will be transferred to the output of the quad D-latches. If LOCAL at terminal 16 of the circuit board connector is low at power-on, the output of U201-12 will remain high and the latch will remain set with U201-16 high and the system in the local mode. If LOCAL at terminals 16 of the connector is high (REMOTE) at power-on, the same sequence of events takes place except that U201-12 will go low after .02 seconds. Thus, the system will power up in the remote mode with the local inputs transferred to the outputs, however, a change in the setting in any of the front panel switches will not result in a change of data at the output terminals of the circuit board. When operating in the remote mode, data will first be applied to the remote inputs and will then be followed by a STROBE pulse at terminal 15 of the circuit board. Since all inputs are ground true, this will cause the latch to be reset with U201 at a low state causing the data selectors to select the remote data. The STROBE pulse will also cause the output of U201-12 to go high to transfer the remote data input to the output of the quad D-latches.

As previously stated, all inputs to the circuit board are ground true. However, the circuit boards to which the outputs of the storage board are connected require a positive true input. Therefore, the $\overline{Q}$ outputs of the quad D-latches are connected to the output terminals of the circuit board.

4.3.2 Positive True-No Storage Logic Board

The schematic diagram of the logic board using positive true logic and without storage is shown in Figure 7.4. The function of the circuitry on this board is simply to select remote or local inputs and connect the selected input to the output terminals. Selection is accomplished through data selectors U201, U205 and U207. The remote inputs to the selectors are positive true and, since the circuits to which the outputs of this circuit board are connected require positive true logic, no inversion of the remote data inputs is made on the circuit board. The local switches on the front panel, however, generate ground true signals which must first be inverted through U201, U204 and U206 before being applied to the inputs of the data selectors. When LOCAL at pin 16 of circuit board connector P2 is high, the inputs from the front panel switches will be connected to the output of the data selectors. When it is low, the remote input data will appear at the output terminals.

4.3.3 Fixed Frequency Oscillator

The schematic diagram for the fixed frequency oscillator is shown in Figure 7-20. Amplifier U601 employs a positive feedback through the 153.6 KHz crystal Y601, and oscillates at the crystal frequency. The output of U601 is divided by a factor of 384 through U603, U604 and U605. A jumper is installed between pins 1 and 12 on the U602 socket to complete the connection between the output of the oscillator and the input of U603. The output of U605 is a 400 Hz square wave. Transistor Q601 driven by U605, produces a standarized square wave that alternates between ground and the zener voltage (6.2 volts). This standarized square wave is then filtered through two stage, four pole, active filter system comprised of the circuits of U608 and U610. The output of the filter is a 400 cycle sine wave with distortion reduced to between 0.1% and 0.15%. This is the AØ oscillator output which is measured at TP601.

The two signals applied to the inputs of U606 have amplitude and phase relationships such, that when combined vectorally, produce the BØ output at U606-6 that lags the AØ by 120^{o}. Note that the circuits comprised of R619, R620 and C607 produce a signal at the non-inverting input of U606 of lesser amplitude than the AØ and which lags the AØ by 30^{o}. A similar circuit produces the CØ output which leads the AØ by 120^{o}. In this case, however, the circuit comprised of C608, R623 and R624 produces a signal at the non-inverting input of U607 that also has reduced amplitude but leads the AØ signal by 30^{o}. An identical circuit to that which produces the CØ output also produces the DØ, or 90^{o} output. However, the signal at the non-inverting input of U609 is adjusted with R627 to produce an output at U609-6 that leads the AØ voltage by 90^{o}. The circuits of U606, U607, and U609 produce output signal amplitudes, irrespective of the phase angle adjustment, that are equal to the AØ amplitude.

4.3.3 Programmable 3Ø Variable Frequency Oscillator

A block diagram of the programmable 3Ø variable frequency oscillator is shown in Figure 4.3.3.1. The BCD input is converted to binary in the code converter. The output of the code converter is applied to the quadrature oscillator. Through a pair of analog-to-digital converters, this input varies the resistance, and therefore the time constant, of the oscillator circuit to adjust the frequency in response to the input command. The range input causes the range switch to introduce additional capacity into the oscillator circuit as the range is lowered. The oscillator develops two outputs that are displaced approximately 90^{o} from one another. These two outputs are summed, in proper proportion, and amplified to produce the CØ output. The resultant CØ output and AØ output are then summed in equal amounts and amplified to produce the BØ output. The AØ and quadrature outputs of the oscillator are also summed, again in the proper proportion to produce the DØ (90^{o}) output.

4.3.3.1 BCD to Binary Code Conversion

Refer to Figure 7.18. The BCD to binary code conversion is accomplished in the binary adders U508, U509, U512 and U513. The "1" bit bypasses these adders and goes directly to the inputs of the digital-to-analog converters. The "2" bit is connected to the A0 input of U509. Therefore, the A0 and B0 inputs to U509 will have a weight of 2 instead of 1. Inputs A1 and B1 will have a weight of 4, inputs A2 and B2 will have a weight of 8 and inputs A3 and B3 will have a weight of 16. The weight of these inputs and the inputs of the other adders are shown in Figure 7.18. Since the adders add binary numbers, each of the BCD inputs is connected to one or more of the adder inputs such that the total weight of the inputs to which it is connected equals the BCD input number. For example the "20" input is connected to the B3 input of U509 which has a weight of 16 and to the B0 input of U508 which has a weight of 4.

The "100" input is connected to the B1 input of U513 which has a weight of 64 and to the B0 input of U513 which has a weight of 32 and is also connected to the C0 input of U508 which will have a weight of 4. Because both inputs to U509, which have a weight of 8, are required for connection to the "10" and "40" inputs, the "8" and "4" inputs are connected through OR gate U510. An "8" input will appear at the A1 input and B1 input of U509. Since these each have a weight of 4, they will be additive to produce an output of 8. A "4" input will appear only at input A1 of U509 and will have the normal weight of 4. If the total weight of the inputs to U509 should exceed 31, the C4 output, terminal 14, will go high loading the weight of 32 into U513. Likewise, if the total of the inputs to U508 exceeds 63, its C4 output will go high loading a weight of 64 into U512. Three of the outputs of U509 are connected to inputs of U508 where they are combined with inputs from the connector and from the S0 output of U513. Similarly three outputs from U513 are connected to inputs of U512 where they are combined with inputs from the connector. The outputs of U508 and U512, along with the S0 output of U509 and the "1" input, are connected to the inputs of the A/D converters. The weight of each of the inputs to the A/D converters is shown in Figure 7.18.

It is necessary to protect the oscillator and the associated power source from an input that would generate a frequency less than 10 Hz. The most significant number in the BCD command code must then be something other than 0. All of the most significant number inputs are connected to an input of NOR gate U514. As long as one of these inputs is high, the B3 input of U513, with the weight of 256, and the B1 input of U512, with a weight of 128, will be held low. Should all of the most significant numbers be missing in the code, the output of U514 will go high loading 384 into the adders to hold the frequency at 384 Hz.

4.3.3.2 Oscillator

A simplified diagram of a quadrature oscillator is shown in Figure 4.3.3.2. This oscillator consists of two integrators, U505 and U504 and a unity-gain inverter stage, U501, forming a negative feedback loop. The effective time constants of

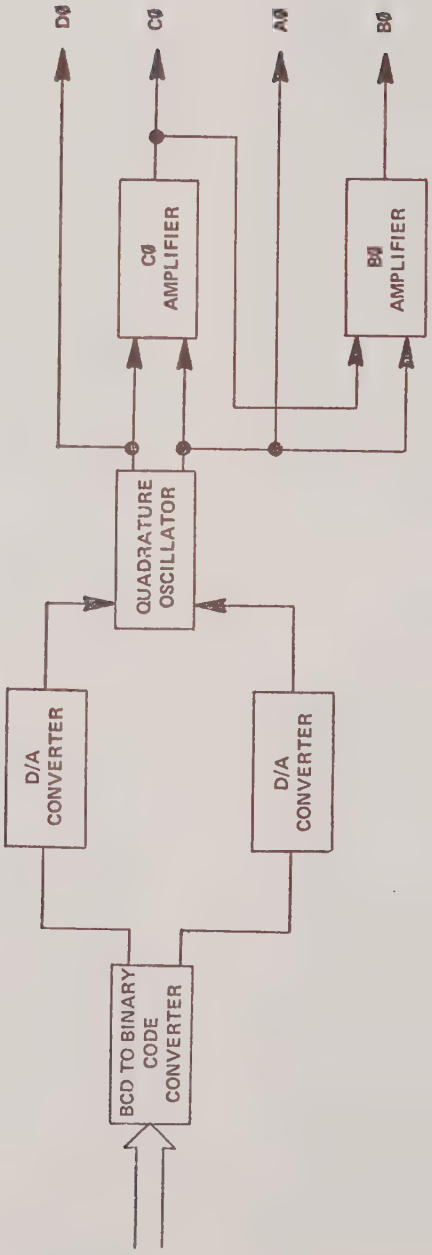


Figure 4.3.3.1. Block Diagram, Programmable 30 Oscillator

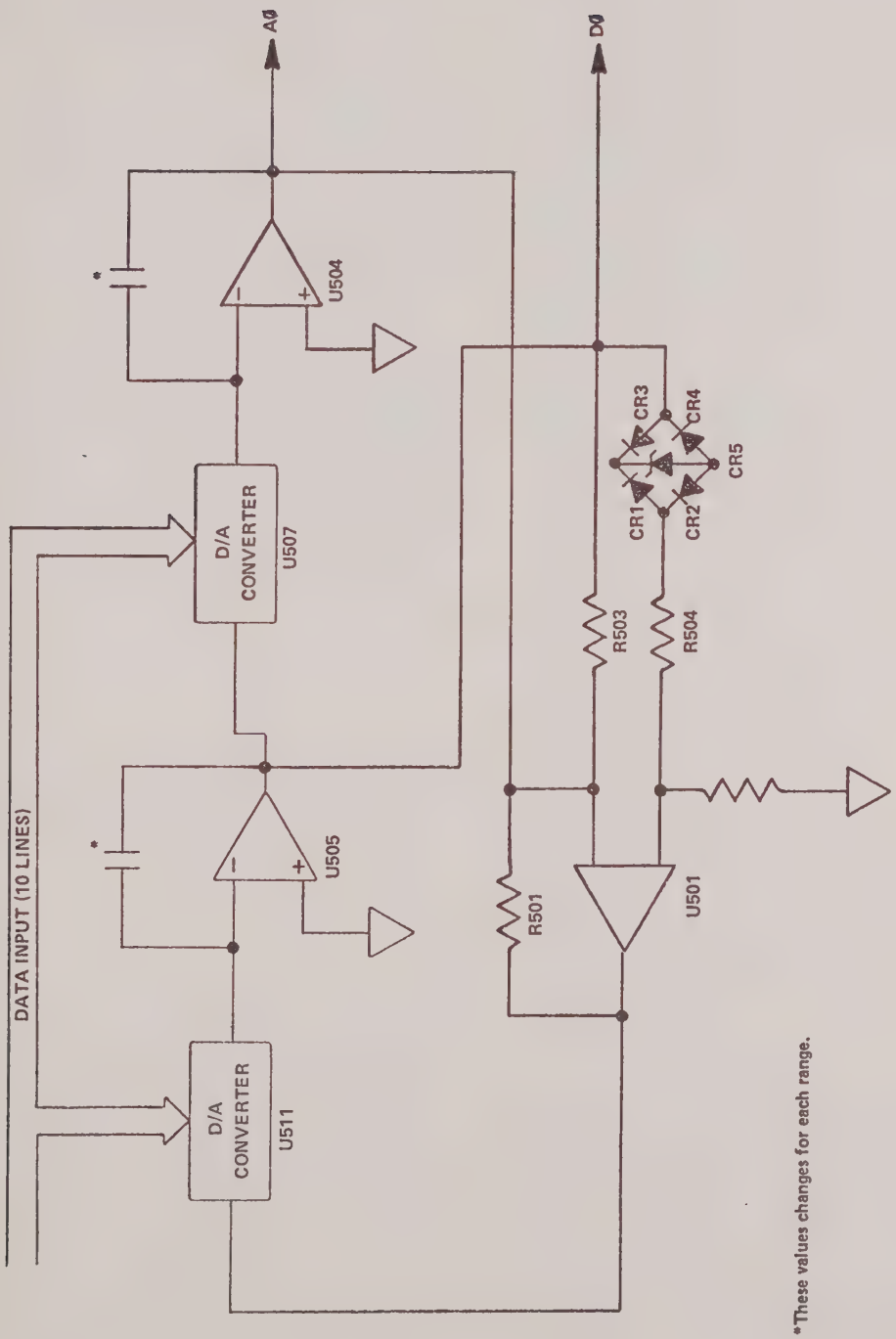


Figure 4.3.3.2. Simplified Circuit Diagram, Quadrature Oscillator

the integrators are varied by the resistance of the D/A converters which is controlled by the binary coded output. The variation of the time constant varies the operating frequency. To insure that oscillations are initiated, positive feedback is introduced from the output of U505 to the input of U501. When the oscillation level has increased to the point where the zener diode conducts at the tips of the wave form, increased negative feedback is introduced through the non-inverting input of U501. Thus, the amplitude of the oscillator is then maintained constant. As previously stated, each of the integrators has a 90^{O} phase lag. Therefore, the output of U505 leads the output of U504 by 90^{O}. This oscillator normally has a practical frequency range of 10 to 1, however, the frequency range requirements of the DAP range from 45 Hz to 9990 Hz (100 to 1). This wide range of frequency, requires that additional capacity be connected across the integrators in the two lower ranges. This is accomplished with quad bilateral switch U506 shown in Figure 7.18. Each of the capacitors identified with the letter "T" in Figure 7.18 is factory selected during calibration to achieve the proper frequency range and tracking.

The outputs of the two integrators are summed at the proper levels at the input of operational amplifier U501 to produce the CØ output which is measured at TP4. The AØ output and the CØ outputs are then summed at equal levels at the input of operational amplifier U501 to produce the BØ output which is measured at TP3.

The digital-to-analog converter resistance ratios are held very close in manufacture. However, the absolute resistance, which in this circuit determines frequency, is not held to close tolerance. Therefore, if a digital-to-analog converter is replaced, it will be necessary to recalibrate the oscillator in accordance with the procedure contained in Section V.

4.3.4 Phase Programmer

A block diagram of the phase converter is shown in Figure 4.3.4.1. The BCD input is converted to binary in the code converter. The output of the code converter is the input to the two phase and amplitude control circuits each comprised of a programmable read-only memory (PROM), a digital-to-analog converter and two operational amplifiers. The outputs of these two circuits are amplitude variable and phase reversible. The output of the sine circuit will have an amplitude equal to the sine of the commanded angle. Its output phase will be 0^{o}, relative to the input reference signal, when the phase angle command is between 271^{o} and 359^{o} and between 0^{o} and 89^{o}. It will be 180^{o}, relative to the input reference signal when the command angle is between 90^{o} and 269^{o}. (At 90^{o} and 270^{o}, the output is zero.) The cosine circuit will have an output amplitude equal to the cosine of the command angle. Its output will be 90^{o}, relative to the AØ signal for angle command from 1^{o} to 179^{o} and 270^{o}, relative to the AØ signal for command angles of 181^{o} to 359^{o}. (At 180^{o} and 0^{o}, the output is zero.)

The output of the two phase and amplitude control circuits are then combined vectorally in another operational amplifier. The output of that amplifier is of constant amplitude with its phase equal to the command phase angle.

4.3.4.1 BCD to Binary Code Conversion

Refer to Figure 7.10. The BCD to binary code conversion is accomplished in digital adders U300, U307, U308 and U309. The "1" bit bypasses these adders and goes directly to the A0 input of both PROM's. The "2" input is connected to the A0 input of U300. Therefore, the A0 and B0 inputs of U300 will have a weight of 2. Inputs A1 and B1 will have a weight of 4, inputs A2 and B2 will have a weight of 8, and inputs A3 and B3 will have a weight of 16. The weight of these inputs and the inputs of the other adders are shown in Figure 7.10. Since the adders add binary numbers, each of the BCD inputs is connected to one or more of the adder inputs such that the total weight of the inputs to which it is connected equals the BCD input number. For example, the "20" input is connected to the B3 input of U300, which has a weight of 16, and to the B0 input of U309, which has a weight of 4. The "100" input is connected to the B1 input of U308, which has a weight of 64, the B0 input of U308 which has a weight of 32 and to the C0 input of U309 which will have a weight of 4. Because the A2 and B2 inputs to U300 are required for the "10" and "40" inputs, the "8" and "4" inputs are connected through OR gate U311. An "8" input will appear at the A1 and B1 inputs of U300. Since both these inputs have a weight of 4, they will be additive to produce an output of 8. A "4" input will appear only at the A1 input of U300 and will have the normal weight of 4. If the total of the inputs to U300 should exceed 31, the C4 output, terminal 14, will go high loading the weight of 32 into U308. Likewise if the total input to U309 exceeds 63, the C4 output will go high loading a weight of 64 into U307. Three of the outputs of U300 are connected to inputs of U309 where they are combined with inputs from the connector and the S0 output of U308. Similarly, the three outputs of U308 are connected to inputs of U307 where they are combined with the "80" input from the connector. The outputs of U307 and U309, along with the S0 output of U300 and the "1" bit input, are connected to the inputs of the two PROM's. Buffering between the adder outputs and PROM inputs is provided to match the CMOS output of the adders to the TTL inputs of the PROM's. Thus, the BCD codes at the input connector are converted to binary codes at the inputs of the PROM's.

4.3.4.2 Phase Control

A simplified diagram of one of the digital-to-analog converters and its associated operational amplifiers is shown in Figure 4.3.4.2. The digital-to-analog converter is represented by two potentiometers in series with the input signal. The potentiometer in series with the same direction to increase the resistance in series with the input to one operational amplifier and to decrease the resistance in series with the input to the other operational amplifier. Operational amplifier U302-7 operates with unity gain and serves as an inverter. The two currents, one from the potentiometer and the

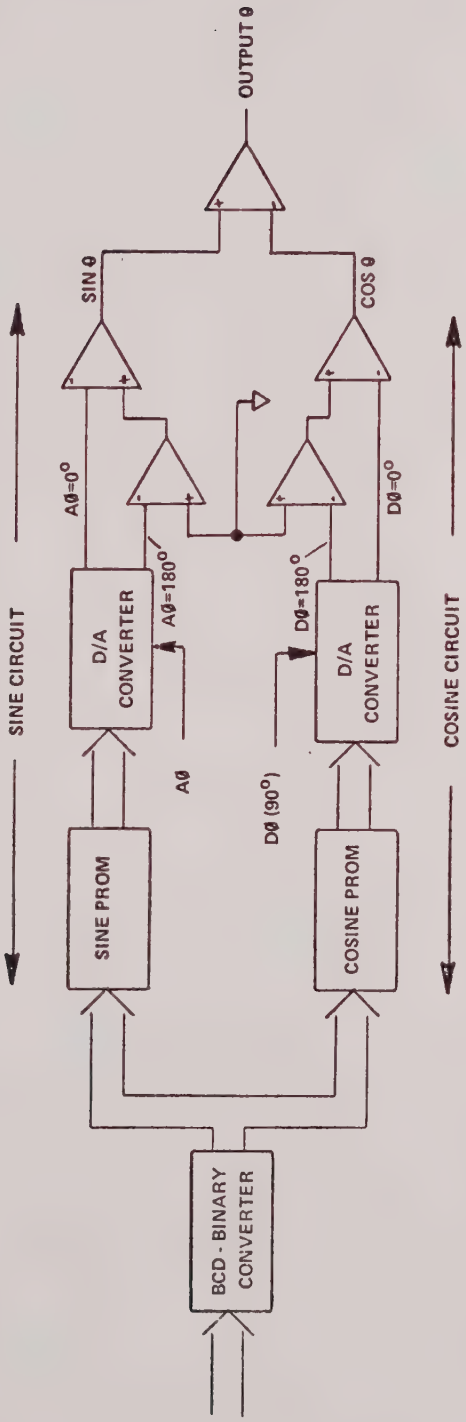


Figure 4.3.4.1. Block Diagram, Phase Programmer

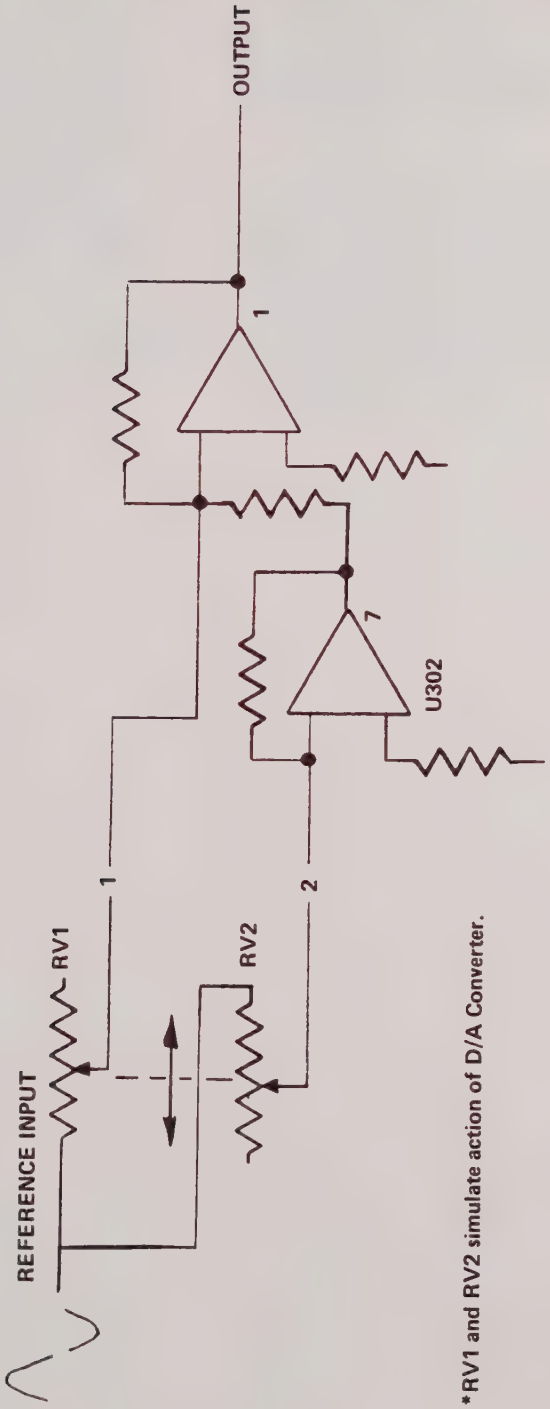


Figure 4.3.4.2. Simplified Circuit Diagram, One-Half of Phase Programmer

other from the output of U302-7, are 180° out of phase. They are applied to the summing junction at the inverting input of U302-1. The output of U302-1 will be in phase with the reference signal when the two potentiometer arms are at the left. As they are moved to the right, the output at U302-1 will decrease becoming zero when they are at mid-point. As the potentiometer arms move further to the right, the output will reverse phase and increase in amplitude reaching maximum when the potentiometer arms are at the extreme right. The outputs of these two circuits then have the amplitude and phase equal to the sine and cosine, respectively, of the command angle.

The sine and cosine outputs are then added vectorally in U301-6. (See Figure 7.10.) The vector addition produces an output from U301-6 that is constant in amplitude for any given angle command and with a phase, relative to the reference AØ that is equal to the command angle.

The PROM's are factory programmed and though they are of the same type, they cannot be interchanged. One is programmed to produce an address to the digital-to-analog converter that will produce the sine output while the other produces an address to the digital-to-analog converter that will produce the cosine output from the same input command code.

4.3.5 130/260 Volt Servo

A block diagram of the 130V/260V Servo circuit board is shown in Figure 4.3.5.1. The function of the servo board is to convert a BCD input command to a voltage level that will drive the output of the associated power source to the command voltage. Aside from the power supply inputs, there are three inputs to this servo board. One input is the oscillator signal which may be obtained directly from the oscillator or from a phase programmer, depending upon the configuration of the DAP in which the servo board is installed. The second input is from the sense transformer which has its primary connected across the load of the power source phase for which the servo provides the driving signal. The third input is the 16 line BCD command bus. The BCD input is converted to binary through the code converter. The output of the code converter is then applied to the input of a multiplying digital-to-analog converter, that functions as a signal attenuator, to attenuate the output of the oscillator amplifier. The attenuator output is then amplified and filtered to provide the driving output voltage. The sense input is rectified in the precision rectifier and compared to the DC output of a second digital-to-analog converter, which is also controlled by the code converter output. The comparison produces an error voltage, which is the difference between the rectified sense voltage and the output of the digital-to-analog converter. This is amplified and filtered and applied to the multiplier which then controls the signal level applied to the input of the amplifier. Ideally the output of the comparator will be zero. Under those conditions the system has a ±10 percent error correcting range.

The transformers for each output leg of the power source has two secondary windings. These may be connected in series to provide the 260 volt range in parallel on the 130 volt range. These windings are connected in series or parallel by relays mounted in the power source and enable the power source to deliver full power on either range. The 260V RGE input, through the amplifier, operates the relays. 260V RGE also operates an analog switch that controls the gain of the output amplifier to change the gain between ranges.

4.3.5.1 BCD to Binary Code Conversion

Refer to Figure 7.12. The BCD to binary code conversion is accomplished in adders U406, U407, U408, U411, U412 and U413. The ".1" bit bypasses these adders and goes directly to the digital-to-analog converters. The ".2" bit is connected to the A1 input of adder U411. Therefore, the A1 and B1 inputs to U411 will have a weight of .2. The A2 and B2 inputs will have a weight of .4, A3 and B3 will have a weight of .8 and A4 and B4 will have the weight of 1.6. The weight of these inputs and the weight of the inputs to the other adders are shown in Figure 7.10. Since the adders sum binary numbers, each of the BCD inputs is connected to one or more of the adder inputs such that the total weight of the inputs to which it is connected equal the BCD input number. For example, the "2.0" input is connected to the B4 input of U411 which has a weight of 1.6 and to the B1 input of U412 which has a weight of .4. The "10" input is connected to the B2 input of U406 which has a weight of 6.4, to the B1 input of U406 which has a weight of 3.2 and to the Ci input of U412 which will have a weight of .4. Because the A3 and B3 inputs of U411 are required for the "1.0" and "4.0" inputs, the ".4" and ".8" inputs are connected through OR gate U410. The ".8" input will appear at both the A2 and B2 inputs of U411. Since both these inputs have a weight of 4, they will be additive to produce an output of .8. A ".4" input will appear only at the A2 input of U411 and will have the normal weight of .4. If the total of the inputs to U411 should exceed 31, the C0 output, terminal 14, will go high, loading the weight of 3.2 into U406. Likewise if the total of the inputs to U412 exceeds 6.3, its C0 output will go high to load the weight of 6.4 into U407. Three of the outputs of U411 are connected to inputs of U412 where they are combined with inputs from the connector and the S1 output of U406. Similarly, three outputs of U406 are connected to inputs of U407 where they are combined with inputs from the connector and the C0 output of U406. Adders U408 and U413 operate from the outputs of U407 and U412 and from inputs from the connector in much the same manner.

OR gate U410 enables the "200" and the

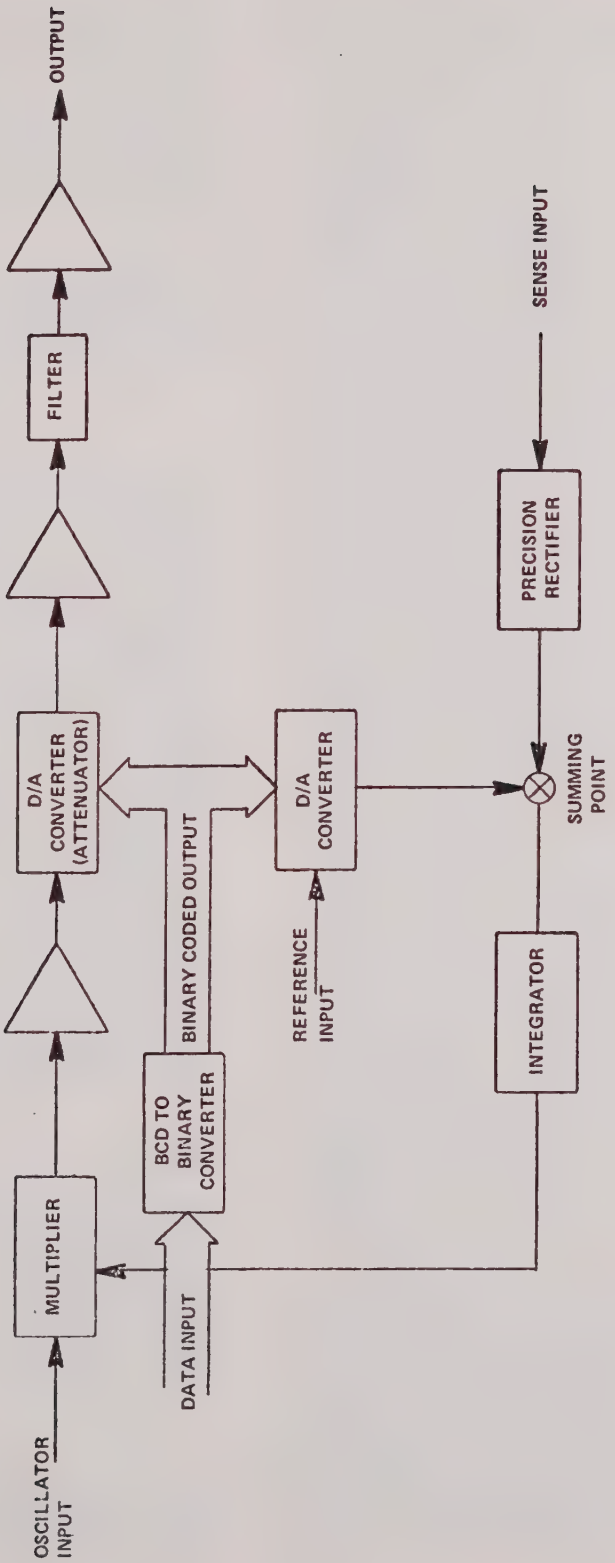


Figure 4.3.5.1. Block Diagram, Servo Circuit Board

"100" inputs to share inputs to adders U408 and U413. This also affords some protection against erroneous input commands. For example, if all input commands were accepted as transmitted, a maximum command of 466.5 would be possible. With the "100" and "200" inputs connected to OR gate U410, the maximum command is 370.5.

The weight of each bit of the code converter output is shown in schematic diagram Figure 7.12. These will be combined, in response to an input, such that their total will equal the BCD input code.

4.3.5.2 Digital-to-Analog Conversion

R401 will normally be adjusted with C408, at the output of the sense integrator, shorted to ground. The adjustment of R401 is then made to produce 260V across the source load with a 260 volt command and 260 volt range input. As the input command is reduced, U403 will introduce a proportional amount of attenuation between the output of U401 and the input of U404. Thus, the output will be reduced proportionately as the command is reduced. A filter, comprised of R407 and C404, is installed between the output of U404 and U405 to filter out the white noise that is introduced by the multiplier, U402. The foregoing adjustment is made based on the predictability of gain in the power source. The output of U405 has a range from 0 to 5 volts. However, the power source input requirement is from 0 to 2 volts. The signal transformer has 5 to 2 step down ratio to accommodate the difference between the output of the servo board and the required input to the power source.

The power source has twice the voltage gain when operating in the 260 volt range as when operating in the 130 volt range. Therefore, the gain of U405 must be reduced by 1/2 when the system is operating in the 260 volt range. This is accomplished by U420 which connects R410 to ground when the 260V RGE signal at terminal K is false.

4.3.5.3 Error Correction

It is, of course, desirable to maintain the commanded voltage at the load terminals with varying loads. The sense rectifier and comparator/integrator will develop an error signal proportional to the change in line voltage drop as the load impedance is varied. This error signal then drives the output of the servo board upward or downward, as necessary, to maintain the commanded voltage across the load terminals. The sense input, at terminal 26 of the circuit board, is developed across a secondary of the sense transformer mounted on the chassis of the DAP. The input signal is rectified in the precision rectifier circuit of U406. U416 has very high and, and very small signals at its input will forward bias the diodes. When the input goes positive, the output goes negative, forward biasing CR402. The junction of R415 and R420 will then follow the output of the amplifier. When the input goes positive, CR402 will be back-biased and CR401 will be forward-biased. The feedback path around U416 tends to maintain its inverting input at, or near, ground potential. Therefore, the voltage at the junction of R415 and R420 will be a series of negative going pulses which is normal for a half wave rectifier. Similarly, a series of positive going pulses are developed at the junction of R414 and R416 and these are inverted through U417. The signal at the output of U417 and that appearing at the junction of R415 and R420, when combined, are equivalent of a full wave rectifier output. These two signals are summed at the input of integrator U418 with the analog output of U415 which is proportional to the command input. The error signal, developed at the output of U414, will be the difference between the rectified sense signal and the analog command signal. This signal is filtered through R423 and C408 and then applied to U401 inversely with the integrator output. This, in turn, varies the overall gain, to compensate for the differences between the command input and the voltage which appears across the load terminals.

Note that digital-to-analog converter U415 requires ground true input logic and that its output will equal approximately 5 volts when the input command is 204.8 volts. Also, U415 is a much more precise analog-to-digital converter than U403. By comparison, U403 provides a coarse adjustment of output voltage. U415, in conjunction with the rectifier and integrator/comparator circuits, provides the precise adjustment of output voltage.

4.3.5 130 Volt Servo

A block diagram of the 130V Servo circuit board is shown in Figure 4.3.5.1. The function of the servo board is to convert a BCD input command to a voltage level that will drive the output of the associated power source to the commanded voltage. Aside from the power supply inputs, there are three inputs to this servo board. One input is the oscillator signal which may be obtained directly from the oscillator or from a phase programmer, depending upon the configuration of the DAP in which the servo board is installed. The second input is from the sense transformer which has its primary connected across the load of the power source phase for which the servo provides the driving signal. The third input is the 16 line BCD command bus. The BCD input is converted to binary through the code converter. The output of the code converter is then applied to the input of a multiplying digital-to-analog converter, that functions as a signal attenuator, to attentuate the output of the oscillator amplifier. The attenuator output is then amplified and filtered to provide the driving output voltage. The sense input is rectified in the precision rectifier and compared to the DC output of a second digital-to-analog converter, which is also controlled by the code converter output. The comparison produces an error voltage, which is the difference between the rectified sense voltage and the output of the digital-to-analog converter. This is amplified and filtered and applied to a mulitplier which then controls the signal level applied to the input of the amplifier. Ideally, the output of the comparator will be zero. Under those conditions the system has a ±10 percent error correcting range.

4.3.5.1 BCD to Binary Code Conversion

Refer to Figure 7.14. The BCD to binary code conversion is accomplished in U406, U407, U408, U411, U412 and U413. The ".1" bit bypasses these adders and goes directly to the digital-to-analog converters. The ".2" bit is connected to the A1 input of adder U411. Therefore, the A1 and B2 inputs to U411 will have a weight of .2. The A2 and B2 inputs will have a weight of .4, A3 and B3 will have a weight of .8 and A4 and B4 will have the weight of 1.6. The weight of these inputs and the weight of the inputs to the other adders are shown in Figure 7.14. Since the adders sum binary numbers, each of the BCD inputs is connected to one or more of the adder inputs such that the total weight of the inputs to which it is connected equal the BCD input number. For example, the "2.0" input is connected to the B4 input of U411 which has a weight of 1.6 and to the B1 input of U412 which has a weight of .4. The "10" input is connected to the B2 input of U406 which has a weight of 6.4, to the B1 input of U406 which has a weight of 3.2 and to the Ci input of U412 which will have a weight of .4. Because the A3 and B3 inputs of U411 are required for the "1.0" and "4.0" inputs, the ".4" and ".8" inputs are connected through OR gate U410. The ".8" input will appear at both the A2 and B2 inputs of U411. Since both these inputs have a weight of 4, they will be additive to produce an output of .8. A ".4" input will appear only at the A2 input of U411 and will have the normal weight of .4. If the total of the inputs to U411 should exceed 31, the C0 output, terminal 14, will go high, loading the weight of 3.2 into U406. Likewise if the total of the inputs to U412 exceeds 6.3, its C0 output will go high to load the weight of 6.4 into U407. Three of the outputs of U411 are connected to inputs of U412 where they are combined with inputs from the connector and the S1 output of U406. Similarly, three outputs of U406 are connected to inputs of U407 where they are combined with inputs from the connector and the C0 output of U406. Adders U408 and U413 operate from the outputs of U407 and U412 and from inputs from the connector in much the same manner.

The weight of each bit of the code converter output is shown in the schematic diagram of Figure 7.14. These will be combined, in response to an input, such that their total will equal the BCD input code.

4.3.5.2 Digital-to-Analog Conversion

R401 will normally be adjusted with C408, at the output of the sense integrator, shorted to ground. The adjustment of R401 is then made to produce 5 volts at the output of U405 with a 130 volt command. As the input command is reduced, U403 will introduce a proportional amount of attentuation between the output of U401 and the input of U404. Thus, the output will be reduced

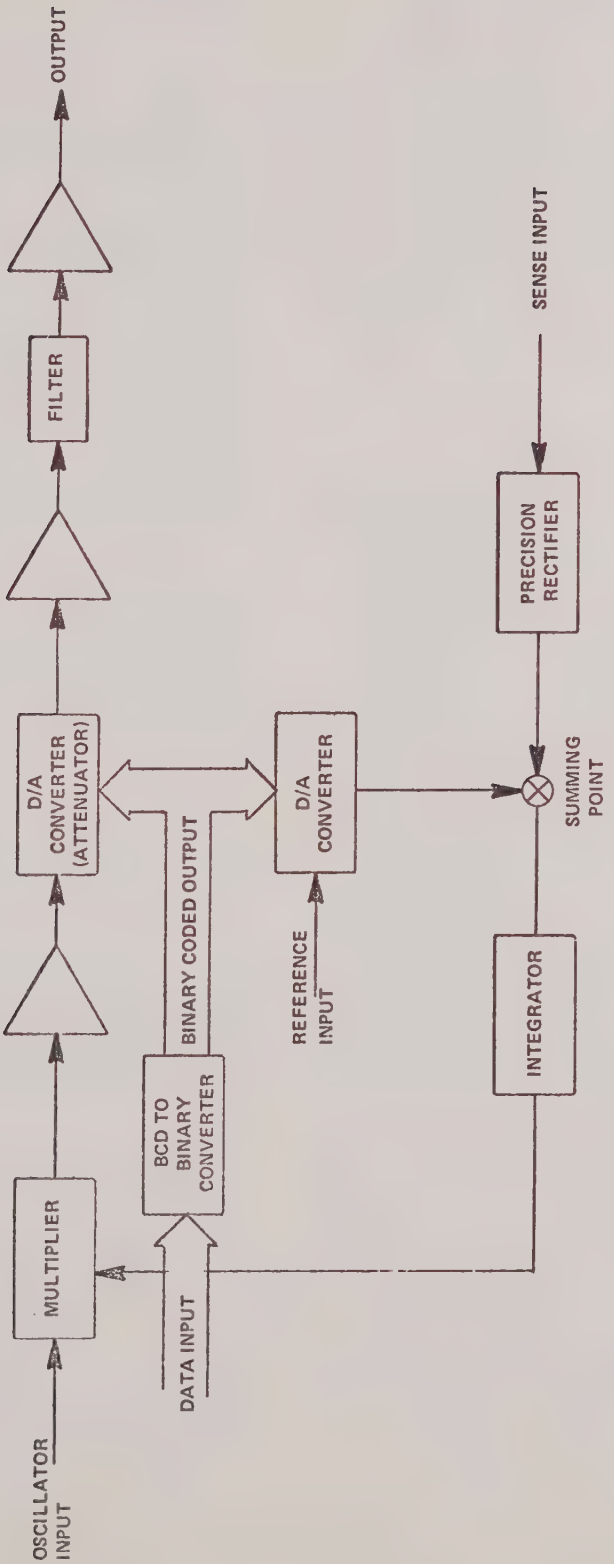


Figure 4.3.5.1. Block Diagram, Servo Circuit Board

proportionately as the command is reduced. A filter, comprised of R407 and C404, is installed between the output of U404 and U405 to filter out the white noise that is introduced by the multiplier U402. The foregoing adjustment is made based on the predictability of gain in the power source. As previously stated, the output of U405 has a range from 0 to 5 volts. However, the power source input requirement is from 0 to 2 volts. The output transformer has a 5 to 2 step down ratio to accommodate the difference between the output of the servo board and the required input to the power source.

4.3.5.3 Error Correction

It is, of course, desirable to maintain the commanded voltage at the load terminals with varying loads. The sense rectifier and comparator/integrator will develop an error signal proportional to the change in line voltage drop as the load impedance is varied. This error signal then drives the output of the servo board upward or downward, as necessary, to maintain the commanded voltage across the load terminals. The sense input, at terminal 16 of the circuit board, is developed across a secondary of the sense transformer mounted on the chassis of the DAP. The input signal is rectified in the precision rectifier circuit of U416. U416 has very high gain and very small signals at its input will forward bias the diodes. When the input goes positive, the output goes negative, forward biasing CR402. The junction of R415 and R420 will then follow the output of the amplifier. When the input goes positive, CR402 will be back-biased and CR401 will be forward-biased. The feedback path around U416 tends to maintain its inverting input at, or near, ground potential. Therefore, the voltage at the junction of R415 and R420 will be a series of negative going pulses which is normal for a half wave rectifier. Similarly, a series of positive going pulses are developed at the junction of R414 and R416 and these are inverted through U417. The signal at the output of U417 and that appearing at the junction of R415 and R420, when combined, are the equivalent of a full wave rectifier output. These two signals are summed at the input of integrator U418 with the analog output of U415 which is proportional to the command input. The error signal, developed at the output of U418, will be the difference between the rectified sense signal and the analog command signal. The signal is filtered through R423 and C408 and then applied to four-quadrant multiplier U402. The transmission between terminals 1 and 4 of U402 varies inversely with the integrator input. This, in turn, varies the gain of the amplifier stage, U401, to compensate for the difference between the command input and the voltage which appears across the load terminals.

Note that digital-to-analog converter U415 requires ground true logic and that its output will equal approximately 2.5 volts when the input command is 102.4 volts. Also, U415 is a much more precise analog-to-digital converter than U403. By comparison, U403 provides a coarse adjustment of output voltage. U415, in conjunction with the rectifier and integrator/comparator circuits, provides the precise adjustment of output voltage.

4.3.6 IEEE Interface

4.3.6.1 Data Inputs

The IEEE interface circuit board accepts inputs from a system controller that employs the IEEE-488 control and data format and converts those inputs to outputs which are acceptable to the logic boards of the DAP. The interface input has sixteen lines. Three of the interface lines, DAV, NRFD and NDAC effect the transfer of each byte of data on the data lines from the controlling computer to the DAP. Five signal lines, ATN, IFC, SRQ, REN and EOI are used to manage an orderly flow of information across the interface. Of these five lines, only ANT, IFC and REN are used by the DAP. The remaining eight input lines are identified as DIO1 through DIO8 and of these, the DAP utilizes only DIO1 through DIO7.

The mnemonics of the six control lines utilized by the DAP have the following significance:

ATN – ATTENTION. For the DAP to accept address input, this input must go true.

DAV – DATA VALID. When the data on the seven data input lines has stabilized, DAV will go true and the data will be accepted by the DAP.

NRFD – NOT READY FOR DATA. This is an output line, that when true, indicates that the DAP cannot accept data. The controlling computer will not transmit data until NRFD goes false.

NDAC – NOT DATA ACCEPTED. This is an output line and it will be true until the DAP has transferred the input data to the output lines of the interface board. The controller will not send an additional message byte until NDAC goes true.

REN – REMOTE ENABLE. Transfer of the DAP control from local to remote occurs when REN goes true, however, it must be transmitted in parallel with ATN, DAV and seven address bits.

IFC – INTERFACE CLEAR. As explained in detail in later paragraphs, the DAP is placed in the listen mode when it receives its discrete address code when ATN and DAV are true. It will remain in the listen mode until it receives an unlisten command. INTERFACE CLEAR is another type of unlisten command that can be sent independently of all other inputs and will clear all devices connected to the IEEE bus from their listen, or talk, mode.

4.3.6.2 Block Diagram

A block diagram of the IEEE interface is shown in Figure 4.3.6.1. The DAP will normally be powered on in the local mode. To gain control of the DAP, the controller must transmit ATN, five address bits directed to the address comparator, two address bits directed to the listen latch and REN and DAV. The address comparator will compare the five address bits with the address selector switch positions and generate MLA (MY LISTENING ADDRESS) if the comparison is valid. When REN and MLA go true, the local/remote latch will be set to the remote condition. When MLA and the two address bits are true, the listen latch is enabled. ATN and DAV will generate ADDR CLK (ADDRESS CLOCK) at the output of the pulse generator. This will clock the listen latch into the listen condition and will cause NRFD to go false and NDAC to go true. The interface is, then, latched in the listening and remote modes and is ready to accept the data inputs. To transmit data, the controller must transmit five serial bytes each containing seven bits of parallel data. The data is in ASCII code. Bits DIO1 and DIO4 correspond to the row designators and bits DIO5 through DIO7 are the column designators as shown in Table 4.3.6.3. The first four bytes transmitted will contain the data, decimal digits 0 through 9, which will be loaded into the four shift registers. The last byte is a letter, A through G, which will strobe the data in the registers into the appropriate logic card storage. The data in the shift registers is in BCD. The strobe outputs are:

ASCII Code Input	Strobe Output
A	A-Phase Amplitude
B	B-Phase Amplitude
C	C-Phase Amplitude
D	B-Phase Phase Angle

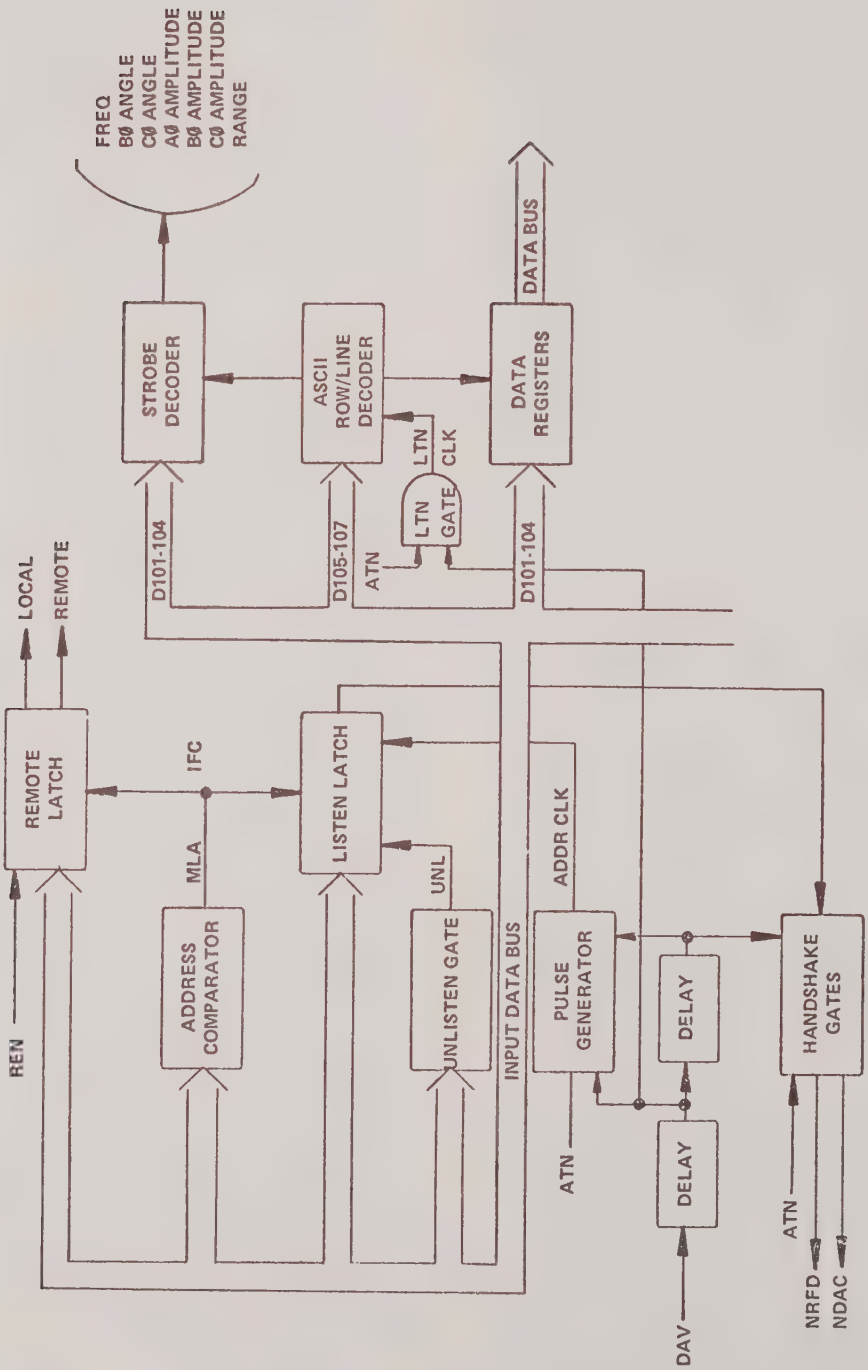


Figure 4.3.6.1. Block Diagram, IEEE-488 Interface Circuit Board

E	A-, B- and C-Phase Amplitudes (Simultaneous)
F	Frequency and Frequency Range
G	C-Phase Phase Angle

Note that when ATN is true, that the pulse generator is enabled to generate the ADDRESS CLOCK. When ATN is false, the listen gate is enabled to generate LTN CLK (LISTEN CLOCK). ATN, therefore, is used to determine the utilization of the information on the data bus. When data is being transmitted, NRFD goes true shortly after DAV goes true and goes false when DAV goes false. NDAC goes false when ADDRESS CLOCK or LISTEN CLOCK goes true and goes false when DAV goes false.

Following the transmission of data, the interface is placed in the unlisten mode so as not to respond to data intended for another device. UNL (UNLISTEN) will go true when the unlisten code is on the data bus and ATN and DAV are true. Thus, the listen latch will be enabled and will be clocked into the unlisten mode when ADDRESS CLOCK goes true. The interface will also be put into the unlisten mode whenever IFC goes true. Thus, the controller can selectively place the DAP in the unlisten mode, or, simultaneously, place all devices on the bus in the unlisten mode by transmitting IFC.

To selectively return the DAP to the local mode, the controller must first transmit the address sequence and then send the GO TO LOCAL byte. The address sequence will set MLA true enabling the remote latch. The GTL (GO TO LOCAL) code on the data bus will trigger the latch to the local condition. The DAP will also return to the local mode whenever REN goes false.

4.3.6.3 Interface Logic

The following paragraphs contain detailed descriptions of the logic circuits of the IEEE interface circuit board, referenced to Figure 7.2. The logic devices on this board of the TTL family. However, all input and output signal lines to this circuit board are ground-true. A number of the signals within the circuit board are positive-true. These are identified in the text. Figure 4.3.6.2 shows the timing relationships within the IEEE interface board.

4.3.6.3.1 Power-On Mode

When power is first applied, the DAP is energized in the unlisten mode so that it will not accept commands from the controller until it has received its discrete address. When power is first applied, R103 and C104 will produce a delay that will maintain the input to Schmitt trigger U106C low for approximately .1 seconds. This forces PON, at the output of U124e, low setting the LISTEN latch comprised of NAND gate U108d and U114b with the output of U114b high. It also resets the LOCAL/REMOTE latch, comprised of NAND U113b and U113a, with the output of U113a high. Therefore, at power on, the DAP is set in the unlisten and local modes.

The output of U114b is connected to one input of U108B and ATN, through receiver U102a, is high at its other input. With ATN false, both inputs to U108b are high, forcing the output of NAND gate U108a, one input of U102d and one input of U101d high. U101d and U102d are OR gates and with either of their inputs high, their outputs, NRFD and NDAC, will be high (false). Note, however, that U101D and U102d are open collector devices and NRFD and NDAC will go false only when all the other devices connected to those lines on the IEEE bus are also false.

4.3.6.3.2 Listen Mode

To be placed in the listen mode, the DAP must receive an address input which matches its discrete address set into address switch assembly S101. For the address to be received, ATN and DAV must be true and the data lines, DIO1 through DIO7, as follows:

$$0\ 1\ A_5\ A_4\ A_3\ A_2\ A_1$$

When ATN goes true, it forces the output of inverter U105C, and one input of NAND gate U112b, high. It also forces the output of U102d (NDAC) low (true). When the address data is stable, DAV will go true forcing the output of inverter U124f, and a second input of U112b, high. Because of the delay introduced by R112 and C102, the

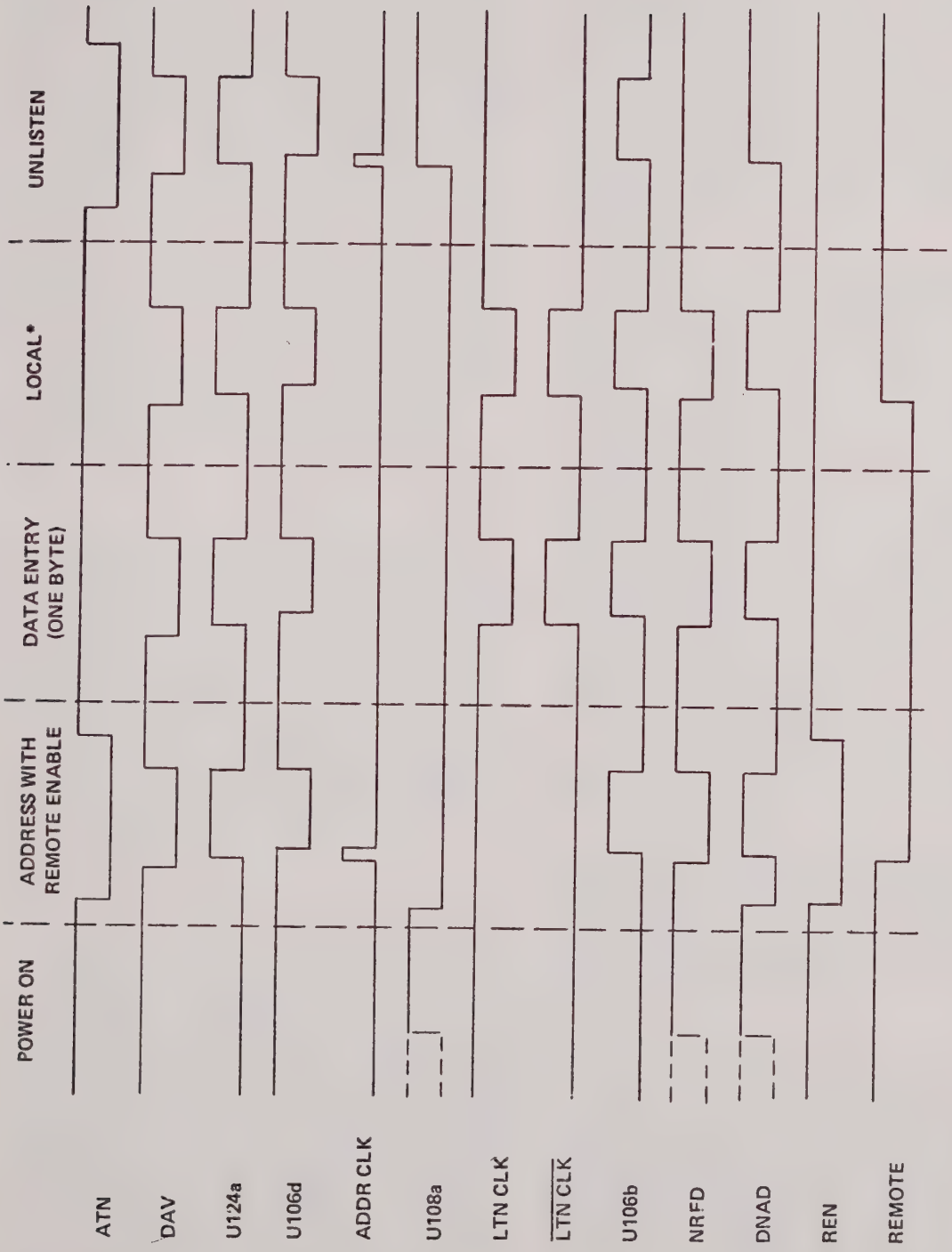


Figure 4.3.6.2. Timing Relationships, IEEE Interface Board

output of inverter U124f will go high approximately .2 microseconds after DAV goes true. Thus, momentarily, all three inputs to NAND gate U112B are high forcing its output low and the output of inverter U107d, and one input of NAND gate U114a, high. Prior to DAV going true, the address bits appeared on the data input lines and were compared in comparator U109 with the inputs from the address switch assembly. If the comparison is valid, the A=B output of U109 will go high creating MLA (MY LISTENING ADDRESS) which is also applied to one input of NAND gate U114a. The address bits on input lines DIO7 and DIO6, which are 0 and 1 respectively, are applied to the inputs of NAND gate U108c, with DIO6 having been inverted through U107e. This forces the output of inverter U107b high. The pulse created at the output of U107d, when DAV goes true, then forces the output of U114a low, setting the LISTEN latch at the output of U110d, LTN (LISTEN), high.

When U124f goes low, it forces the output of U106d low, and the output of U102D (NDAC) high indicating that the DAP has accepted the data. When the LISTEN latch is set, the output of U108a, $\overline{LTN + ATN}$ goes low. The output of U106d is also low and this forces the output of U101d (NFRD) low indicating that the DAP is not ready to accept data. When DAV goes false, the output of U106d goes high forcing NRDF high and NDAC low. The time relationships between the various signals involved in the listen/address mode are shown in Figure 4.3.6.2.

4.3.6.4 Data Entry Mode

To receive data, the IEEE interface board must first receive an address as described in the previous paragraphs. LTN at the output of NAND gate U108d is then high, enabling NAND gate U112c. When a data byte is to be received, ATN will be false making one of the inputs of U112c high. When DAV goes low, indicating that the data is stabilized, the output of converter U124f will be forced high forcing the output of U112C low. Through inverter U124b, AND gates U116a and U116b are enabled. The data that appears on the input lines for a magnitude command correspond to the ASCII codes for column 3 rows 0 through 9 as shown in Figure 4.3.6.3. The code for column three is bit 5=1, bit 6=1, and bit 7=0 the column code will appear on input lines DIO5, DIO6 and DIO7. When the codes on those lines are 1, 1, 0, the output of AND gate U116a will go high to clock the data on line DIO1, DIO2, DIO3 and DIO4 into the first cell of the shift registers. When the data has been clocked in, NDAC will go high indicating that the data has been accepted and the controller can then move on to transmitting the next byte. This sequence will be repeated four times until the shift registers are completely filled with the data from all four bytes.

The data stored in the shift registers will not be utilized in the DAP until a steering pulse from the output of BCD to decimal decoder U117, or from one of the three gates connected to its outputs, is generated. The steering data transmitted by the controller, will conform to the ASCII codes of column 4, rows 1 through 4 and 7 through 9. The code for column 4 is bit 5=0, bit 6=0 and bit 7=1, when this code appears on input lines DIO5, DIO6 and DIO7, the output of U116b will go high enabling AND gates U115a, b, c and d. These will pass the bits of data on input lines DIO1, DIO2, DIO3 and DIO4 to the BCD tó decimal decoder, U117. U117 will decode the BCD input and energize the appropriate output line. The energized output line is an address to one of the individual logic boards of the DAP and it will load the data stored in the shift registers, U120 through U123, into the storage logic of the addressed logic board.

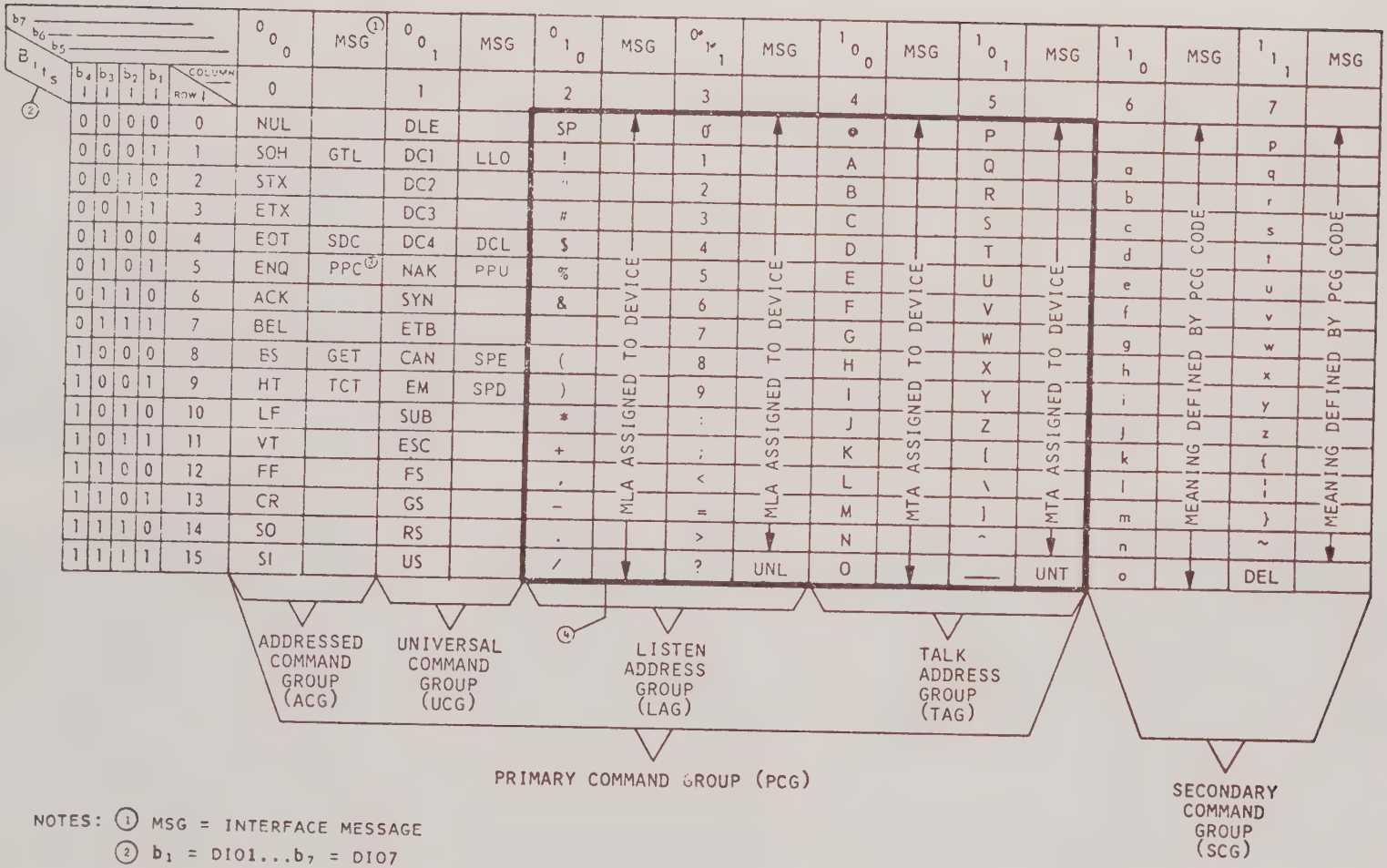
When the foregoing sequence has been completed, a similar sequence, to load data for entry into another logic board, may be initiated immediately. Thus, the controller may load all of the data required for all of the logic boards in the DAP after sending a single address code.

4.3.6.5 Remote Enable Mode

The listen and data entry modes described in the previous paragraphs command the same sequence of events within the IEEE interface whether the DAP is operating in the remote or the local mode. However, because of the logic circuitry, the data transmitted would not load into the storage devices on the logic boards if the unit is in the local mode. It is necessary, therefore, that the controller send a command to put the DAP into the remote mode of

MULTILINE INTERFACE MESSAGES: ISO-7 BIT CODE REPRESENTATION

(SENT AND RECEIVED WITH ATN=1)


b7
b6
b5
Bits
b4 b3 b2 b1
COLUMN
ROW
0 0 0
MSG (1)
0 0 1
MSG
0 1 0
MSG
0 1 1
MSG
1 0 0
MSG
1 0 1
MSG
1 1 0
MSG
1 1 1
MSG
0 0 0 0 0 NUL
0 0 0 1 1 SOH GTL
0 0 1 0 2 STX
0 0 1 1 3 ETX
0 1 0 0 4 EOT SDC
0 1 0 1 5 ENQ PPC (3)
0 1 1 0 6 ACK
0 1 1 1 7 BEL
1 0 0 0 8 BS GET
1 0 0 1 9 HT TCT
1 0 1 0 10 LF
1 0 1 1 11 VT
1 1 0 0 12 FF
1 1 0 1 13 CR
1 1 1 0 14 SO
1 1 1 1 15 SI
0 0 1 DLE
DC1 LLO
DC2
DC3
DC4 DCL
NAK PPU
SYN
ETB
CAN SPE
EM SPD
SUB
ESC
FS
GS
RS
US
2 SP ! " # $ % & ( ) * + , - . /
3 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
4 @ A B C D E F G H I J K L M N O
5 P Q R S T U V W X Y Z [\ ] ^ _
6 a b c d e f g h i j k l m n o
7 p q r s t u v w x y z { | } ~ DEL
MLA ASSIGNED TO DEVICE
MLA ASSIGNED TO DEVICE
UNL
MTA ASSIGNED TO DEVICE
MTA ASSIGNED TO DEVICE
UNT
MEANING DEFINED BY PCG CODE
MEANING DEFINED BY PCG CODE
(2)
(4)
ADDRESSED COMMAND GROUP (ACG)
UNIVERSAL COMMAND GROUP (UCG)
LISTEN ADDRESS GROUP (LAG)
TALK ADDRESS GROUP (TAG)
PRIMARY COMMAND GROUP (PCG)
SECONDARY COMMAND GROUP (SCG)

NOTES: (1) MSG = INTERFACE MESSAGE
(2) b_1 = DIO1...b_7 = DIO7
(3) REQUIRES SECONDARY COMMAND
(4) DENSE SUBSET (COLUMN 2 THROUGH 5)

Figure 4.3.6.3 ASCII Code Chart

operation before sending command data. This would certainly be necessary before the first set of commands in-as-much as the DAP powers up in the local mode. To put the DAP in the remote mode, it is only required that REMOTE ENABLE be true when the address code is transmitted. The address code will set MLA (MY LISTEN ADDRESS), and one input to NAND gate U112a, high. REMOTE ENABLE will force the output of inverter U107E, and another input of U112a, high. The address clock pulse will then force the output of U112a low setting the latch, comprised of U113b and U113a, with the output of U113b high and the output of U113a low which is the condition for remote operation of the DAP.

The normal mode of operation is remote. Therefore, REN is normally true. However, GTL (GO TO LOCAL) maybe transmitted and the DAP will respond although REN is true.

To return the system to the local mode, the controller must first go through the step of transmitting the address. It then follows with the data code of bit DIO1=1 and all other bits at "0" and with DAV low. The input bits are applied to NAND gate U111. Note that DIO1 is inverted in U105b. When DAV goes true, it generates LISTEN CLOCK at the output of NAND gates U112C which forces the output of inverter U124b, and the remaining input to U111, high. This forces the output of U111, GTL, low resetting the latch with the output of U113b low which is the condition for local control of the DAP.

4.3.6.6 Unlisten Command

When the controller has completed its data transmission to the DAP, it must transmit an unlisten command to reset the listen latch of U108d and U114b. The unlisten command is the ASCII code for "7" and is the same for all devices on the bus. It requires that ATN and DAV be true, that DIO1 be true and DIO2 through DIO7 false. DIO1 is inverted in U105b, thus all inputs to NAND gate U110, with exception of input 4, are high. When DAV goes low, it generates the address clock which is applied to input 4 of U110 to force its output, UNL, low resetting the listen latch. This returns the IEEE interface board circuitry to the same condition as when power was first applied except that the LOCAL/REMOTE latch is not affected.

4.3.7 LOCAL CONTROL INPUT SWITCHES

Local control of the DAP is accomplished with up to six sets of pushbutton rotary switches and a REMOTE/LOCAL toggle switch. When the REMOTE/LOCAL switch is in the LOCAL position, the control of the DAP and the AC Power Source is accomplished with the front panel mounted pushbutton rotary switches. Each of the six functions of a fully configured DAP (frequency, phase angle and amplitude programming for three output phases) may be controlled with these switches. The switches are digital, ten-position types that produce BCD, ground-true inputs to their individual logic boards. The four switches that control frequency include a range switch with X1/10, X1 and X10 positions. The digital readout of the three switches to its left will be multiplied by the display on the range switch. Thus, switch settings of 450 X1/10 will produce an output frequency of 45 Hz. The switches for the phase angle programmers enable the local control of phase angle in 1^{o} steps from 000^{o} to 399^{o}, although settings from 000^{o} to 359^{o} are normally used. The switches for the amplitude programmers enable the local control of output amplitude in 0.1V steps from 000.5V to 130V (or 130/260V). The switch to the logic board connections are shown in Figure 7.1.

When Options 1 or 2 and Option 5 (Parallel BCD Inputs and Local Control respectively) are installed, a REMOTE/LOCAL switch will be installed. This switch holds the LOCAL line, terminal 16 on the logic board, (refer to Figure 7.1) low when in the LOCAL position. (The LOCAL line may also be held low by the controller input.) This forces the outputs of NAND gates U201-12 and U201-6 high. Quad latches U206, U207, U208 and U209 are, then, held in a condition where their outputs follow their inputs. Data selectors U202, U203, U204 and U205 then have their outputs connected to the inputs that are connected to the individual switches in each group. This provides direct control of the output of the latches from the front panel switches. In this condition, the output of the latches follow the positions of the switches.

When the DAP is configured with Option 1 or 2 and Option 5, and the remote input is disconnected

from the DAP or the input is disabled from strobing the latches, the data entered with the panel switches may be stored at the output of the quad latches by placing the REMOTE/LOCAL switch in the REMOTE position. New data may then be set in with the panel switches without affecting the output until the REMOTE/LOCAL switch is returned to the LOCAL position. The new data will then control the output of the DAP. This is a particularly useful feature when it is desired to program all outputs to a predetermined level simultaneously since they can be set individually without affecting the output then simultaneously entered with the REMOTE/LOCAL switch. This feature is possible since, when the LOCAL line goes high with the REMOTE/LOCAL switch in the REMOTE position, the data at the input of the quad latches is stored at their outputs regardless of the state of their inputs.

4.3.8 COMMAND DISPLAY

The commands, whether originating from a remote or a local source, are displayed on the front panel by groups of seven-segment, LED digital displays. The commands, as stored on the logic boards and produced at their output in BCD, positive-true logic, are decoded by seven-segment decoder/drivers, U1 through U22 as shown in Figure 7.1. The seven-segment displays are of the common anode type and the decoder-drivers provide the supply source for each segment in accordance with the input code to provide the appropriate digit display. Decimal point displays for the three amplitude command displays are permanently connected to ground through a fixed resistor. The decimal point for the frequency readout is decoded by U4. The input and output coding for U4 is:

Range Switch Setting	Inputs		Outputs	
	Pin 1	Pin 7	Pin 10	Pin 11
X10	0	0	1	1
X1	0	1	1	0
X1/10	1	0	0	1

Note that pins 2, 5 and 6 of U4 are grounded. With all inputs (1-2-6-7) grounded, the output normally go to "0", however, the ripple blanking input, pin 5, is also grounded causing all outputs to go to the "1" state when all inputs are "0". Therefore the decimal points are blanked when the range switch is at X10 and individually selected when it is in the X1 or X1/10 position. Note that the decimal point in the next most significant digit display will light when the switch is in the X1/10 position and the one in the next least significant digit display will light when it is in the X1 position. The series limiting resistors are contained in U23 through U44 except for those associated with decimal points.

Note that the displays are of the commands and not of the output generated in response to commands.

4.3.9 POWER SUPPLIES

The schematic diagram for the power supply is shown in Figure 7.1. Actually, there are three rectifier - filter - regulator sources in the DAP, and these can be referred to as power supplies although they all obtain their input from a common transformer. CR12 and CR13 comprise one source and they supply unfiltered and unregulated power to the command displays, if displays are installed. The second source rectifies the input AC through CR9 and CR10. The resultant DC is filtered by C11 and regulated by Q9 and Q10 which are connected as a Darlington amplifier with the base voltage determined by CR11. C12 provides a low impedance path to ground from the output. The output is at +5V and supplies the power for all the logic devices in the DAP.

The third power source provides +15V and −15V for the operational amplifiers. The AC from the transformer is full-wave rectified by CR3, CR4, CR5 and CR6 which are connected as a bridge. The transformer center tap is the common return point for this, and the other two power supplies. The output of the bridge rectifier is filtered by C5, C6, C8 and C9. The positive regulator is comprised of Q1, Q2, Q3 and Q4 and associated components. When power is first applied, CR7 supplies current to zener diode CR8 and the base of Q3. Q3 and Q4 are connected as a differential amplifier. When Q3 is first turned on, it turns on Q1 and Q2. Current for CR8 is then furnished through Q2 and R10. If the output rises above +15V, Q4 will draw more current and the current through Q3 will be reduced, in turn, reducing the current through Q1 and Q2. If the output drops below +15V, the opposite condition will occur to cause Q2 to pass more current

and maintain the output at +15V. The negative voltage supply uses a similar circuit, however, rather than a zener diode providing the reference, it is furnished by the voltage divider connected between +15V and −15V output lines. C7 and C10 provide the necessary low impedance path from the +15V and −15V supply lines and the common return.

SECTION V
MAINTENANCE

5.1 GENERAL

This section of the manual contains procedures for verification of performance, disassembly, troubleshooting and adjustment of the DAP Digital Decoder Programmer. The DAP is delivered with all adjustments and calibrations completed. Further adjustment should not be required unless a malfunction occurs or certain critical parts are replaced.

If the procedures of this section and the circuit descriptions of Section IV do not provide sufficient information to locate and correct a malfunction, the assistance of the Elgar Service Department should be requested. Equipment should not be returned to the Elgar factory without the express authorization of Elgar Corporation or its appointed representative. Elgar cannot assume responsibility for equipment returned without authorization.

5.2 REQUIRED TEST EQUIPMENT

The equipment required to conduct the performance verification procedures and for troubleshooting are listed in Table 5.1. Where the listed item of equipment is not available, substitute equipment may be employed provided that such equipment meets the accuracy specifications of the listed item.

5.3 DISASSEMBLY

All integrated circuit devices on the plug-in circuit boards are installed in sockets and may be removed and replaced using any of a number of tools available for that purpose. Circuit board connectors and components of the power supplies and some components on the plug-in boards are soldered in place and are removed and replaced using soldering techniques appropriate to printed circuit boards.

NOTE

Use a low-temperature soldering iron and a vacuum solder removal tool when removing and replacing components soldered to a printed circuit board. Avoid prolonged application of heat to the solder terminal so as to avoid separation of the solder pad from the glass/epoxy substrate.

5.3.1 Cover Removal

The top and bottom covers of the DAP are removed by removing the eight screws that attach the cover to the side and rear channels of the chassis.

NOTE

The DAP is powered from 117V AC or 230V AC. These voltages are dangerous to life. Avoid contact with the Power switch on the front panel and terminal strip at the right rear corner of the unit when the covers are removed.

5.3.2 Circuit Board Removal

The several plug-in circuit boards may be removed when the DAP Power is OFF. Remove

TABLE 5.1 REQUIRED TEST EQUIPMENT

NAME	MANUFACTURER AND PART NUMBER	USE
Differential Voltmeter	John Fluke Mfg. Co., Seattle, Washington (FSC 89536) Model 931	Amplitude test and adjustments; troubleshooting
Frequency Counter	Weston Instruments, Inc., Archbald, Pa. (FSC 94271) Model 302	Frequency test and adjustments; oscillator troubleshooting
Multimeter	Simpson Electric Co., Chicago, Illinois Model 260	Continuity checking; troubleshooting; power supply test
DP Series Simulator	Elgar Corporation, San Diego, California Model DP Simulator	Functional and specification checkout
Oscilloscope	Tektronix, Inc., Beaverton, Oregon Model 561	Signal tracing; phase-angle verification; troubleshooting
Dual-trace Plug-in	Tektronix, Inc., Model 3A6	Signal tracing; phase-angle verification; troubleshooting
Autotransformer	General Radio Co., West Concord, Mass. (FAC 24655) Model VARIAC	Decoder programmer checkout and troubleshooting
Signal Generator	Hewlett Packard, Palo Alto, California Model 200CD	Decoder programmer troubleshooting

boards by grasping the top covers between thumb and forefinger and gently rocking the board while exerting upward pressure. Circuit boards are indexed such that they can be inserted only in the proper connectors. Note that the logic board, phase programmer boards and amplitude programmer boards are interchangeable with a board of the same type. This feature will prove helpful when troubleshooting a malfunction.

5.3.3 Power Supply Access

Access to replace some of the power supply components may require that the sense input and/or signal output transformers be removed. The sense input transformers are mounted on the rear chassis channel with 6-32 screws, nuts and No. 6 lockwashers. The hardware may be removed and the harness assembly has sufficient slack that the transformers may be lifted clear to provide access to power supply components. The signal output transformers are mounted on the circuit board guide. The transformers and guide can be removed by removing two 8-32 screws through each chassis side channel and three 8-32 screws that attach the mother board to the circuit board guide. It will be necessary to remove all plug-in circuit boards before removing the guide and transformers.

5.3.4 Command Display Removal

To gain access to the seven-segment LED command displays, it is necessary to remove the two Phillips head screws that attach the front panel handles. The front panel is then free to be lifted up and rearward. The displays are made up of individual seven-segment LED units, mounted in sockets that may be individually removed and replaced.

5.3.5 Pushbutton Rotary Switch Replacement

The pushbutton rotary, local control switches may be replaced as individual units. It will first be necessary to remove the entire assembly of switches which will require unsoldering the black wire that makes the common ground connection between the two multiple switch assemblies. The bus wire is then cut at each side of the individual defective switch and the other wires to the individual switch removed. Note and mark each wire with the switch terminal number to which it is connected. Next, remove the two 4-40 nuts on one end of the multiple switch assembly and withdraw the threaded wire that holds the assembly together and remove the defective switch.

The replacement switch is installed using the reverse procedure, however, jumper wires must be installed to complete the ground connection where the section of bus wires was removed.

5.4 PERIODIC INSPECTION

Whenever the DAP Digital Decoder Programmer is removed for maintenance, or at six months intervals, it should be thoroughly inspected to insure that it is not returned to service in a marginal condition.

1. Inspect all front panel controls for ease of operation, broken switch buttons or levers, cracked or badly scratched display lenses or loose attaching hardware.

2. Check circuit boards for evidence of component overheating, cracked substrate, loose solder joints. Check that all integrated circuits are firmly seated in their sockets.

3. Check security of hardware that attaches the sense input and signal output transformers to the chassis.

4. Check security of hardware that attaches the power transformer and the cable connectors to the rear panel.

5. If command displays are installed, check each one for burned out elements or elements that produce low level light output.

6. Remove any accumulation of dust or other foreign material with a vacuum cleaner or a soft brush and a low velocity air source. Be certain that, when using pressurized air, that the foreign material is blown clear and is not lodged elsewhere in the unit.

5.5 ADJUSTMENTS

There are only a few adjustments that must be made in the DAP Digital Decoder Programmer. These are made at the factory and should not require readjustment unless critical components are replaced. The function of these adjustments and the manner in which they are made is covered in the following paragraphs.

5.5.1 Frequency Programmer Adjustment

The operating frequency of the three-phase, variable frequency oscillator is determined by the absolute value of the internal resistors of the digital-to-analog (D/A) converters and the total capacity of the individual integrators. The D/A converter internal resistances are not maintained with precision during manufacturing, although they are quite stable with temperature and time. Therefore, replacement of a D/A converter requires that the integrator capacitance be trimmed to bring the operating frequencies within tolerance. It is also necessary that the integrator capacitance be trimmed to adjust the amplitude of the AØ and DØ outputs to be exactly equal. Adjustments are made with the circuit board plugged into the DAP. Refer to Figure 7.7 for location of components and adjustment location.

5.5.1.1 Adjustment Procedure

NOTE

Replacement of either of the type AD7531 digital-to-analog converters will necessitate readjustment of the programmable 3Ø oscillator in accordance with the following procedure.

1. If the oscillator requires adjustment because of replacement of a D/A converter, capacitors C501, C503, C505, C508, C509, C512, C519 through C524 must first be removed from the circuit board.

2. Set C516 and C517 to their capacitive midpoint.

3. Connect a pair of precision capacitor decade boxes with 0-1000 picofarad range across C502 and C504 using very short leads.

4. Connect a frequency meter to TP4 on the oscillator circuit board and a phase meter between TP2 and TP4.

5. Turn the DAP Power Switch to ON and program the oscillator for 9990 Hz.

6. Set both capacitor decade boxes to zero.

7. Increase the capacity at the terminals of each decade box by the same amount until the reading of the frequency meter is 9900 ±1 Hz.

8. Check the reading of the phase meter which should read 240° ±0.5° (lag) and 120° ±0.5° (lead).

9. If the phase meter reading is not within limits, decrement the capacity at the terminals of one decade box by 10 picofarad and increment the capacity of the other by the same amount. Recheck the phase meter reading. (If the phase angle error has increased, the wrong decade box has been decremented. Return both boxes to the same settings before proceeding to decrement the correct decade box.)

10. Continue to decrement one decade box in 10 picofarad steps and increment the other decade box in 10 picofarad steps until the phase meter reading is within the above specified limits or where it is within the range of adjustment with C516 and C517 (±200 Hz or ±0.5°).

11. Install fixed capacitors in the positions of C503 and C519, in combination, that will equal the capacity inserted with the decade box connected across C504.

12. Install fixed capacitors in the positions of C501 and C520, in combination, that will equal the capacity inserted with the decade box connected across C502.

13. Adjust C516 and C517 to trim the frequency and phase angle errors within specified limits.

NOTE

The adjustment of C516, to bring the phase angle within limits will result in a frequency shift that will require correction by adjustment of C517 (or vice versa). Since these two adjustments are interactive, the proper procedure is to make a small adjustment of one in the direction to correct, say, a phase error, but do not attempt to completely correct the error. Adjust the other capacitor to correct the frequency shift caused by the first adjustment. Make another small adjustment for phase error correction, a small one for frequency, etc., until the final adjustment is achieved.

14. Program the frequency for 999.0 Hz and connect the capacitor decade boxes across C507 and C511.

15. Repeat steps 6 through 12 for a frequency meter reading of 999.0 Hz ± 5 Hz and phase angles of 120° ± 0.5°. However, the capacitors to replace the capacity of the decade box connected across C507 will be installed at the positions for C508 and C522 and those for the decade box connected across C511 at the positions for C512 and C524.

16. Program the frequency for 99.9 Hz and connect the capacitor decade boxes across C506 and C510.

17. Repeat steps 6 through 12 for a frequency meter reading of 99.9 Hz ± .5 Hz and phase angles of 120° ±0.5° and 240° ±0.5°. However, the capacitors to replace the capacity of the decade box connected across C506 will be installed at the positions for C505 and C523 and those for the decade

box connected across C510 at the positions for C509 and C521.

5.5.2 Servo Adjustment

The servo system operation is dependent on the gain of the AC Power Source. For this reason, the servo adjustment requires that the DAP and AC Power Source be connected as a system with the sense input leads connected across the load, if a load is connected to the AC Power Source output. Refer to Figure 7.11 for location of components and adjustment.

5.5.2.1 Adjustment Procedure

1. Turn the DAP and AC Power Source Power switches to OFF.

2. Connect a clip lead across C408 on each installed servo board.

3. If a load is connected to the AC Power Source output, the sense input lines to the DAP should be connected across that load. Also, the load should not be subject to damage when the AC Power Source output is full scale (150V or 260V) or at 10% of full scale (15V or 26V).

4. Connect a digital voltmeter across the AØ output of the AC Power Source.

5. Turn the AC Power Source Power switch ON and the DAP Power switch ON.

6. Program the DAP for the frequency and output phase angles appropriate to the load.

7. Program the DAP for full scale output voltage from the AC Power Source (130V or 260V) as appropriate.

8. Adjust R401 on each servo board for full scale output voltage ±1V as read on the digital voltmeter.

9. Disconnect the clip lead across C408 on each installed servo board.

10. Adjust R411 on each servo board for full scale output voltage ±.05V as read on the digital voltmeter.

11. Program the DAP for 10% of full scale output voltage from the AC Power Source.

12. Adjust R418 for 10% of full scale output voltage ±.05V as read on the digital voltmeter.

13. Reprogram full scale output.

14. R411 and R418 will interact. Therefore, repeat steps 10 through 13 until further adjustment is not required.

5.6 PERFORMANCE VERIFICATION

The DAP Digital Decoder Programmer should have its performance verified at six-month intervals. The performance verification procedure can be accomplished with the DAP connected in the system and with the necessary precision test equipment listed in Table 5.1 connected as directed in the following paragraphs. The procedure checks oscillator frequency, phase angle output and amplitude output over the operating range.

5.6.1 Preliminary Set-Up

Before starting the performance verification check, verify the following:

1. DAP Power switch at OFF.

2. AC Power Source Power switch at OFF.

3. Program source de-energized or in standby condition.

4. Any load disconnected from the AC Power Source.

5.6.2 Local Mode Check

Performance of the DAP can be verified in the local mode using the front panel pushbutton rotary switches for command input. The following procedure assumes a fully configured DAP with frequency, phase angle and amplitude programming.

If the unit is equipped with input command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit the steps for those functions not included in the DAP under test.

Proceed as follows to verify performance of the DAP in the LOCAL mode:

1. Place the REMOTE/LOCAL switch in the LOCAL position.

2. Set all AMPLITUDE switches to zero.

3. Connect the frequency meter between the HI and LO test posts on the front panel of the AC Power Source and the differential voltmeter across one phase output of the AC Power Source.

4. Connect the phase meter between the AØ and BØ outputs of the AC Power Source.

5. Set the FREQUENCY switches to 450 X1/10.

6. Place the AC Power Source Power switch in the ON position , then the DAP Power switch in the ON position.

7. Verify that the differential voltmeter reads less than 500 mv. Check all three output phases of the AC Power Source.

8. Set the BØ ANGLE switches to 120^{o} and the CØ ANGLE switches to 240^{o}.

9. Set the amplitude switches to 120.

10. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the output of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120V $\pm$ 0.2 V.

11. Verify that the BØ angle is $120^{o} \pm 1^{o}$. Connect the phase meter between the AØ and CØ outputs of the AC Power Source and verify that the CØ angle is $240^{o} \pm 1^{o}$.

12. If the DAP and the AC Power Source are configured for 130V/260V, set the AMPLITUDE switches to 240.

13. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the output of all three phases of the AC Power Source, as read on the differential voltmeter, are at 240V $\pm$ .2 V.

14. Verify that the phase angles have remained at $120^{o} \pm 1^{o}$ and at $240^{o} \pm 1^{o}$.

15. Set the AMPLITUDE switches to 012 (024 if the DAP and AC Power Source are configured for 130V/260V).

16. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 12 V $\pm$ 0.2 V (24V $\pm$ 0.5 V if the DAP and AC Power Source are configured for 130V/260V).

17. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

18. Set the AMPLITUDE switches to 120 and the FREQUENCY switches to 450 X1.

19. Verify that the frequency meter reads 450 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120V $\pm$ 0.2 V.

20. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

21. Set the FREQUENCY switches to 450 X10.

22. Verify that the frequency meter reads 4500 Hz $\pm$ 22.5 Hz and that the outputs of all three phases of the AC Power Source are at 120V $\pm$ 0.2 V.

23. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

24. Set the FREQUENCY switches to 999 X10.

box connected across C510 at the positions for C509 and C521.

5.5.2 Servo Adjustment

The servo system operation is dependent on the gain of the AC Power Source. For this reason, the servo adjustment requires that the DAP and AC Power Source be connected as a system with the sense input leads connected across the load, if a load is connected to the AC Power Source output. Refer to Figure 7.15 for location of components and adjustment.

5.5.2.1 Adjustment Procedure

1. Turn the DAP and AC Power Source Power switches to OFF.
2. Connect a clip lead across C408 on each installed servo board.
3. If a load is connected to the AC Power Source output, the sense input lines to the DAP should be connected across that load. Also, the load should not be subject to damage when the AC Power Source output is full scale (150V or 260V) or at 10% of full scale (15V or 26V).
4. Connect a digital voltmeter across the AØ output of the AC Power Source.
5. Turn the AC Power Source Power switch ON and the DAP Power switch ON.
6. Program the DAP for the frequency and output phase angles appropriate to the load.
7. Program the DAP for full scale output voltage from the AC Power Source (130V or 260V) as appropriate.
8. Adjust R401 on each servo board for full scale output voltage ±1V as read on the digital voltmeter.
9. Disconnect the clip lead across C408 on each installed servo board.
10. Adjust R411 on each servo board for full scale output voltage ±.05V as read on the digital voltmeter.
11. Program the DAP for 10% of full scale output voltage from the AC Power Source.
12. Adjust R418 for 10% of full scale output voltage ±.05V as read on the digital voltmeter.
13. Reprogram full scale output.
14. R411 and R418 will interact. Therefore, repeat steps 10 through 13 until further adjustment is not required.

5.6 PERFORMANCE VERIFICATION

The DAP Digital Decoder Programmer should have its performance verified at six-month intervals. The performance verification procedure can be accomplished with the DAP connected in the system and with the necessary precision test equipment listed in Table 5.1 connected as directed in the following paragraphs. The procedure checks oscillator frequency, phase angle output and amplitude output over the operating range.

5.6.1 Preliminary Set-Up

Before starting the performance verification check, verify the following:

1. DAP Power switch at OFF.
2. AC Power Source Power switch at OFF.
3. Program source de-energized or in standby condition.
4. Any load disconnected from the AC Power Source.

5.6.2 Local Mode Check

Performance of the DAP can be verified in the local mode using the front panel pushbutton rotary switches for command input. The following procedure assumes a fully configured DAP with frequency, phase angle and amplitude programming.

If the unit is equipped with input command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit the steps for those functions not included in the DAP under test.

Proceed as follows to verify performance of the DAP in the LOCAL mode:

1. Place the REMOTE/LOCAL switch in the LOCAL position.

2. Set all AMPLITUDE switches to zero.

3. Connect the frequency meter between the HI and LO test posts on the front panel of the AC Power Source and the differential voltmeter across one phase output of the AC Power Source.

4. Connect the phase meter between the AØ and BØ outputs of the AC Power Source.

5. Set the FREQUENCY switches to 450 X1/10.

6. Place the AC Power Source Power switch in the ON position , then the DAP Power switch in the ON position.

7. Verify that the differential voltmeter reads less than 500 mv. Check all three output phases of the AC Power Source.

8. Set the BØ ANGLE switches to 120^{o} and the CØ ANGLE switches to 240^{o}.

9. Set the amplitude switches to 120.

10. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the output of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120V $\pm$ 0.2 V.

11. Verify that the BØ angle is $120^{o} \pm 1^{o}$. Connect the phase meter between the AØ and CØ outputs of the AC Power Source and verify that the CØ angle is $240^{o} \pm 1^{o}$.

12. If the DAP and the AC Power Source are configured for 130V/260V, set the AMPLITUDE switches to 240.

13. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the output of all three phases of the AC Power Source, as read on the differential voltmeter, are at 240V $\pm$ .2 V.

14. Verify that the phase angles have remained at $120^{o} \pm 1^{o}$ and at $240^{o} \pm 1^{o}$.

15. Set the AMPLITUDE switches to 012 (024 if the DAP and AC Power Source are configured for 130V/260V).

16. Verify that the frequency meter reads 45 Hz $\pm$ 0.225 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 12 V $\pm$ 0.2 V (24V $\pm$ 0.5 V if the DAP and AC Power Source are configured for 130V/260V).

17. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

18. Set the AMPLITUDE switches to 120 and the FREQUENCY switches to 450 X1.

19. Verify that the frequency meter reads 450 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120V $\pm$ 0.2 V.

20. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

21. Set the FREQUENCY switches to 450 X10.

22. Verify that the frequency meter reads 4500 Hz $\pm$ 22.5 Hz and that the outputs of all three phases of the AC Power Source are at 120V $\pm$ 0.2 V.

23. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

24. Set the FREQUENCY switches to 999 X10.

25. Verify that the frequency meter reads 9990 Hz ± 50 Hz and that the outputs of all three phases of the AC Power Source are at 120V ± 0.2 V.

26. Verify that the BØ angle is 120° ±1° and the CØ angle is 240° ±1°.

27. Set the FREQUENCY switches to 450 X1, the BØ ANGLE switches to 045 and the CØ ANGLE switches to 045.

28. Verify that the BØ and CØ output phase angles are at 45° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

29. Set the BØ ANGLE and CØ ANGLE switches to 180.

30. Verify that the BØ and CØ output phase angles are 180° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

31. Set the BØ ANGLE and CØ ANGLE switches to 270.

32. Verify that the BØ and CØ output phase angles are 270° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

33. Set the BØ ANGLE and CØ ANGLE switches to 000.

34. Verify that the BØ and CØ output phase angles are 000° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

35. Set the AMPLITUDE switches to 000.

36. Turn the DAP and AC Power Source Power switches to OFF.

37. Test is complete.

If any deviation from the limits specified above is observed during the performance verification check, the system should be checked to determine if the DAP or AC Power Source is malfunctioning. If the DAP is found to be the cause of the deviations, normal troubleshooting procedures should be employed to determine the cause of the malfunction. Refer to the adjustment and troubleshooting paragraphs of this section for information on correction of the observed problem.

5.6.3 Remote Mode Check (IEEE-488 Interface)

The remote mode check consists of programming the frequency, amplitude and phase angle inputs of the DAP to several values within the range of each function. If a test program is available in the controller, the AC Power Source outputs can be recorded and the test may be accomplished automatically. If a test program is not available, programming in accordance with that detailed in Section III must be devised and entered through the rear panel connector, J103.

The following procedure assumes a fully configured DAP with frequency, phase angle and independent amplitude programming, as well as local control. If the unit is equipped with command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit the steps for those functions not included in the DAP under test.

1. Verify that the Power switches on both the AC Power Source and the DAP are in the OFF position.

2. Connect the program source to the rear panel connector, J103 on the rear panel of the DAP.

3. Connect the digital frequency meter to the output test posts on the front panel of the AC Power Source. Also, connect a differential voltmeter between the AØ output and common connection of the AC Power Source.

4. Connect a phase meter between the AØ and BØ outputs of the AC Power Source.

5. Place the AMPLITUDE switches on the front panel of the DAP to 000.

6. Place the Power switch on the AC Power Source at ON then place the Power switch on the DAP at ON.

7. Verify that the differential voltmeter reading is less than 500 mv. Check all three outputs of the AC Power Source.

8. Program REMOTE and then program the frequency to 45 Hz, the BØ angle to 120^{o}, the CØ angle to 240^{o} and all amplitudes to 120V.

9. Verify that the digital frequency meter reads 45 Hz ±0.45 Hz, and that the outputs of all three phases of the AC Power Source, as read with the differential voltmeter, are at 120V ±1V.

10. Verify that the BØ angle is $120^{o} \pm 1^{o}$. Verify that the CØ angle is $240^{o} \pm 1^{o}$ by connecting the phase meter between the AØ and CØ outputs of the AC Power Source.

11. If the DAP and the AC Power Source are configured for 130V/260V, program the amplitude for 240V.

12. Verify that the frequency meter reads 45 Hz ±0.45 Hz and that the outputs of all three phases of the AC Power Source, as read on the differential voltmeter, are at 240V ± 0.5V.

13. Verify that the phase angles have remained at $120^{o} \pm 1^{o}$ and $240^{o} \pm 1^{o}$.

14. Program the amplitude to 12V (24V if the DAP and AC Power Source are configured for 130V/260V).

15. Verify that the frequency meter reads 45 Hz ± 0.225 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 12V ± 0.2 V (24V ± 0.5 V if the DAP and the AC Power Source are configured for 130V/260V).

16. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

17. Program the amplitude to 120V and the frequency to 450 Hz.

18. Verify that the frequency meter reads 450 Hz ± 2.25 Hz and that the outputs of all three phases of the AC Power Source, as measured on the differential voltmeter, are at 120 V ± 0.2 V.

19. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

20. Program the frequency to 4500 Hz.

21. Verify that the frequency meter reads 4500 Hz ± 22.5 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2 V.

22. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

23. Program the frequency to 9990 Hz.

24. Verify that the frequency meter reads 9990 Hz ± 50 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2V.

25. Verify that the BØ angle is $120^{o} \pm 1^{o}$ and the CØ angle is $240^{o} \pm 1^{o}$.

26. Program the frequency for 450 Hz, the BØ angle for 45^{o} and the CØ angle for 45^{o}.

27. Verify that the BØ and CØ output phase angles are at $45^{o} \pm 1^{o}$ and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2 V.

28. Program the BØ and CØ angles to 180^{o}.

29. Verify that the BØ and CØ output phase angles are $180^{o} \pm 1^{o}$ and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2V.

30. Program the BØ and CØ angles to 270^{o}.

31. Verify that the BØ and CØ output phase angles are at 270° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

32. Program the BØ and CØ angles to 000°.

33. Verify that the BØ and CØ output phase angles are at 000° ±1° and that the outputs of all three phases of the AC Power Source are at 120V ± 0.2V.

34. Program all amplitudes to 000.

35. Turn the DAP Power switch and the AC Power Source Power switch to OFF.

36. Test is complete.

If any deviation from the limits specified above is observed during the performance verification check, the system should be checked to determine if the DAP, AC Power Source or controller is malfunctioning. If the DAP is found to be the cause of the deviations, normal troubleshooting procedures should be employed to determine the cause of the malfunction. Refer to the adjustment and troubleshooting paragraphs of this section for information on correction of the observed problem.

5.6.4 Remote Mode Check (16 Line BCD Coded Input)

The remote mode check consists of programming the frequency, amplitude and phase angle inputs of the DAP to several values within the range of each function. If a test program is available in the controller, the AC Power Source outputs can be recorded and the test may be accomplished automatically. If a test program is not available, programming in accordance with that detailed in Section III must be devised and entered through the rear panel connector, J103.

The following procedure assumes a fully configured DAP with frequency, phase angle and independent amplitude programming, as well as local control. If the unit is equipped with command displays, those displays should be checked at every step in the procedure to assure that they coincide with the program input. Omit the steps for those functions not included in the DAP under test.

1. Verify that the Power switches on both the AC Power Source and the DAP are in the OFF position. Also, place the DAP REMOTE/LOCAL switch in the REMOTE position.

2. Connect the program source to the rear panel connector, J103 on the rear panel of the DAP.

3. Connect the digital frequency meter to the output test posts on the front panel of the AC Power Source. Also, connect a differential voltmeter between the AØ output and common connection of the AC Power Source.

4. Connect a phase meter between the AØ and BØ outputs of the AC Power Source.

5. Place the AMPLITUDE switches on the front panel of the DAP to 000.

6. Place the Power switch on the AC Power Source at ON then place the Power switch on the DAP at ON.

7. Verify that the differential voltmeter reading is less than 500 mv. Check all three outputs of the AC Power Source.

8. Program the frequency command input to the DAP to 45 Hz, the BØ angle to 120°, the CØ angle to 240° and all three amplitudes to 120.

9. Verify that the digital frequency meter reads 45 Hz ± 0.225 Hz, and that the outputs of all three phases of the AC Power Source, as read with the differential voltmeter, are at 120 V ± 0.2 V.

10. Verify that the BØ angle is 120° ±1°. Verify that the CØ angle is 240° ±1° by connecting the phase meter between the AØ and CØ outputs of the AC Power Source.

11. If the DAP and the AC Power Source are configured for 130V/260V, program the amplitude for 240V.

12. Verify that the frequency meter reads 45 Hz ± 0.225 Hz and that the outputs of all three phases of the AC Power Source, as read on the differential voltmeter, are at 240 V ± 0.5 V.

13. Verify that the phase angles have remained at 120° ±1° and 240° ±1°.

14. Program the amplitude to 12V (24V if the DAP and AC Power Source are configured for 130V/260V).

15. Verify that the frequency meter reads 45 Hz ± 0.225 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 12 V ± 0.2V (24V ± 0.5 V if the DAP and AC Power Source are configured for 130V/260V).

16. Verify that the BØ angle is 120° ±1° and the CØ angle is 240° ±1°.

17. Program the amplitude to 120V and the frequency to 450 Hz.

18. Verify that the frequency meter reads 450 Hz ± 2.25 Hz and that the outputs of all three phases of the AC Power Source, as measured on the differential voltmeter, are at 120 V ± 0.2 V.

19. Verify that the BØ angle is 120° ±1° and the CØ angle is 240° ±1°.

20. Program the frequency to 4500 Hz.

21. Verify that the frequency meter reads 4500 Hz ± 22.5 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2 V.

22. Verify that the BØ angle is 120° ±1° and the CØ angle is 240° ±1°.

23. Program the frequency to 9990 Hz.

24. Verify that the frequency meter reads 9990 Hz ± 50 Hz and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2V.

25. Verify that the BØ angle is 120° ±1° and the CØ angle is 240° ±1°.

26. Program the frequency for 450 Hz, the BØ angle for 45° and the CØ angle for 45°.

27. Verify that the BØ and CØ output phase angles are at 45° ±1° and that the outputs of all three phases of the AC Power Source, as measured with the differential voltmeter, are at 120 V ± 0.2 V.

28. Program the BØ and CØ angles to 180°.

29. Verify that the BØ and CØ output phase angles are 180° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

30. Program the BØ and CØ angles to 270°.

31. Verify that the BØ and CØ output phase angles are at 270° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

32. Program the BØ and CØ angles to 000°.

33. Verify that the BØ and CØ output phase angles are at 000° ±1° and that the outputs of all three phases of the AC Power Source are at 120 V ± 0.2 V.

34. Program all amplitudes to 000.

35. Turn the DAP Power switch and the AC Power Source Power switch to OFF.

36. Test is complete.

If any deviation from the limits specified above is observed during the performance verification check, the system should be checked to determine if the DAP, AC Power Source or controller is malfunctioning. If the DAP is found to be the cause of the deviations, normal troubleshooting procedures should be employed to determine the

cause of the malfunction. Refer to the adjustment and troubleshooting paragraphs of this section for information on correction of the observed problem.

5.7 TROUBLESHOOTING

Because the design of the DAP is straightforward, there are no special troubleshooting procedures required. A thorough study of the Theory of Operation, Section IV is a prerequisite to efficient servicing of the DAP. When the operation of the circuits is understood, the observed symptoms will suggest the procedure to use in determining which circuit, or device, is malfunctioning. The test equipment required for troubleshooting is listed in Table 5.1. In any event, the DAP will need to be connected to the AC Power Source when troubleshooting the servo boards. It can stand alone when troubleshooting the logic boards, frequency oscillator and phase programmers. Table 5.2 lists a number of symptoms and some of the malfunctions which can cause them. It is not possible to predict all failure modes of the many devices used in the DAP, and the described symptoms may be generated by failure modes that are unanticipated. Therefore, if the suggested remedy does not solve the problem, it will be necessary to analyze the problem more thoroughly and the technician will be on his own for the most part. If the problem is not solved within a reasonable time, request the assistance of the Elgar Service Department. The personnel there may have experienced the same problem and may have a solution for it that does not appear in this manual. If not, they may be able to suggest an approach to solving the problem and, as a last resort, can authorize the return of the unit to Elgar for service. Equipment should never be returned without such authorization as Elgar dislcaims reponsibility for equipment shipped to it without such prior authorization.

The logic boards are interchangeable as are the phase programming boards and the servo boards. Interchanging of boards is a logical first step in troubleshooting the system since this can determine if the trouble is within the DAP or in some other unit of the system. It can also determine if the trouble is the fault of a failed transformer in the case of a servo system malfunction. If it has been determined, for example, that the AC Power Source is operating correctly and interchanging the servo board does not correct a problem existing in only one phase, a transformer could be suspect and should be checked out.

5.8 POWER SUPPLY CHECK

Whenever a malfunction occurs, the possibility of a power supply malfunction should not be overlooked. The proper functioning of the power supply can be checked as follows:

1. Connect a DC voltmeter between the red and black test points in the area of the power supply. Measure +15V ±1.5V.

2. Connect a DC voltmeter between the green and black test points. Measure −15V ±1.5V.

3. Connect a DC voltmeter between the orange and black test points. Measure +5V ±0.5V.

If the measured voltage(s) are not within the limits specified above, the power supply should be analyzed and repaired before attempting to correct another malfunction. However, the possibility of the other malfunction contributing to the power supply being out of limits should not be overlooked.

TABLE 5.2. TROUBLESHOOTING CHART

Symptom	Possible Cause
Overvoltage (approximately 10%) on one phase.	1. Open sense transformer. 2. Defective precision rectifier component. 3. Defective multiplier, U402. 4. Defective D/A converter, U403 or U415.
Undervoltage on one phase.	1. Defective precision rectifier component. 2. Defective multiplier, U402. 3. Defective D/A converter, U403 or U415. 4. Defective latch on logic board. 5. Defective selector on logic board. 6. Defective adder on servo board.
Zero output on one phase.	1. Defective NAND gate on logic board preventing latches from storing input data. 2. Defective amplifier, U401, U404 or U405. 3. Defective A/D converter, U403.
Incorrect output on all phases.	1. Defective IEEE interface board. 2. Defective input connector (16 line BCD input). 3. Defective IEEE interface board connector.
Incorrect phase programmer output.	1. Defective IEEE interface board. 2. Defective IEEE interface board connector. 3. Defective input connector (16 line BCD input). 4. Defective adder on programmer board. 5. Defective latch on logic board. 6. Defective selector on logic board. 7. Defective A/D converter on programmer board, U303 or U304. 8. Defective amplifier on programmer board, U301 or U302. 9. Defective PROM, U305 or U306.
Zero output from 3Ø programmable oscillator.	1. Defective amplifier, U504, U505 or U501. 2. Defective A/D converter, U507 or U511. 3. Shorted CR5 on programmer board. 4. Defective amplifier U501.
Does not shift frequency to X1/10 or X1 range.	1. Defective switch, U506.

TABLE 5.2 TROUBLESHOOTING CHART (Continued)

Symptom	Possible Cause
Incorrect frequency output on any range.	1. Defective A/D converter, U507 or U511. 2. Defective adder, U508, U509, U512 or U513. 3. Defective OR gate U510. 4. Defective integrating capacitor in U504 or U505 circuit.
Phase error in BØ, CØ and DØ outputs.	1. Defective A/D converter, U507 or U511. 2. Defective A/D converter replaced and oscillator not recalibrated. (See 5.5) 3. Defective integrating capacitor in U504 or U505 circuit.
Phase error in BØ output only.	1. Defective resistor in U501-14 circuit. 2. Defective U501-14.
Phase error in DØ output only.	1. Defective R512 or R513. 2. Defective U501-7.
Phase error in BØ and CØ output only.	1. Defective R506 or R507. 2. Defective U501-8.
Fixed Frequency Oscillator operates on wrong frequency.	1. Defective crystal, Y601. 2. Defective divider, U603, U604 or U605. 3. R605 installed in wrong position.
Outputs non-sinusoidal.	1. Defective component in active filter circuit of U608 and U610. 2. Open CR601.
Output voltage in excess of normal 5V RMS.	1. Open CR601.
Phase error in one output.	1. Phase shifter circuit needs adjustment. 2. Defective resistor in amplifier feedback circuit. 3. Defective capacitor in adjustment circuit.
Input accepted by wrong logic board.	1. Defective AND gate, U115a, U115b, U115c or U115d, producing improper output for BCD to decimal decoder, U117. 2. Defective BCD to decimal decoder, U117.
Input data not transferred to logic board.	1. Defective AND gate, U115 or U116b. 2. Defective BCD to decimal decoder, U117. 3. Defective NAND gate, U119.

TABLE 5.2. TROUBLESHOOTING CHART (Continued)

Symptom	Possible Cause
Does not respond to address input.	1. Address switch set improperly or defective switch. 2. Defective comparator, U109. 3. Defective NAND gate U114a. 4. Defective NAND gate U112b. 5. Defective inverter, Z103b, Z105d, Z107b, or Z124f. 6. Defective NAND gate, U108d or U114b. 7. Defective Schmitt trigger, U106a, U106d. 8. Defective CR102 or CR103. 9. Defective C103, C101.
Input data not stored in registers on IEEE interface board but strobe pulse developed.	1. Defective AND gate U116a.
LISTEN indicator lighted but system will not go into remote mode.	1. Defective NAND gate in remote latch. 2. REN receiver defective. 3. Defective inverter U103c. 4. Defective NAND gate U112a.
LISTEN and REMOTE indicators lighted. Unit does not respond to input.	1. Defective NAND gate U112c. 2. Defective inverter U104b. 3. Defective AND gate U116a or U116b.
Does not respond to UNL command.	1. Defective NAND gate, U111.
Does not power up in local mode.	1. Defective component in power up circuit of U106c and U124e.
No response to input.	1. Defective line receiver.

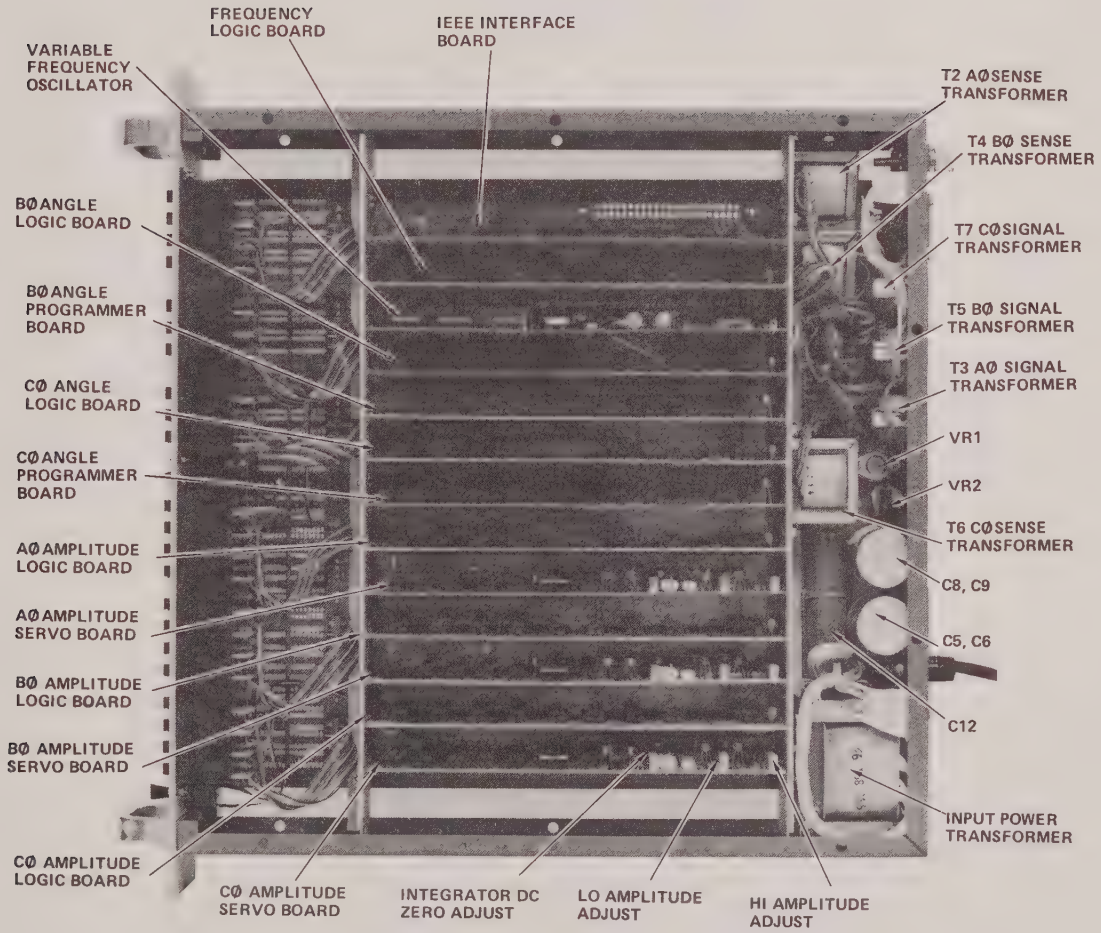


Figure 5.1. DAP Inside View

SECTION VI
PARTS LISTS

6.1 GENERAL

6.2 This section contains a listing of all parts necessary for factory-authorized repair of the Elgar Decoder Programmer. Location of parts and assemblies are given on an assembly drawing accompanying each board schematic. Parts are located on the assembly drawing and correlated on the parts lists by reference designators. Note that trimming capacitors are factory-selected parts and replacement of these parts is beyond the scope of customer maintenance. They are, therefore, not included in the following lists.

6.3 When ordering spare parts, specify part name, part number, manufacturer, component value and rating. Where no specific manufacturer or part number is given, the replacement part should conform to value, rating, and tolerance as listed. If complete assemblies are desired, order assemblies from Elgar Corporation, 8225 Mercury Ct., San Diego, CA 92111. Specify assembly number, instrument series number and instrument name.

DAP CHASSIS ASSEMBLY

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER NAME	MANUFACTURER PART NUMBER	ELGAR PART NUMBER
C5,6,8,9	2x1000uF	Capacitor	25 V	Mallory	PWP201. 15A	824-108-52
C7	0.1 uF	Capacitor	35 V	Sprague	196104X9035HA1	823-104-61
C10	1 uF	Capacitor	35 V	Sprague	196D105X0353A1	823-105-61
C11	10,000uF	Capacitor	10 V	Sprague	39D109G010JT4	824-109-22
C12	220 uF	Capacitor	10 V	Sprague	196D227X0010MA3	823-227-61
CR3, 10,12, 13		Diode		Motorola	1N4004	845-400-4X
CR7		Diode		T.I.	1N914	844-914-XX
CR11		Zener Diode		Motorola	MZ500-12	842-500-12
Q2		NPN Transistor		RCA	40250V1	839-402-5V
Q1		NPN Transistor		Fairchild	2N3567	835-356-7X
R2	1 K	Resistor	½W,5%	Speer	RC20GF102J	802-102-05
R1	.22	Resistor, W.W.	5W,5%	Dale	CW5.22	807-R22-05
T1		Power Xfmr		Elgar		990-801-93
T2,4, 6		Sense Xfmr		Elgar		990-717-9X
T3,5,7		Signal Xmfr		Elgar		990-718-9X
VR1		Voltage Regulator	+15 V	Motorola	7815 ACP	849-781-5P
VR2		Voltage Regulator	−15 V	Motorola	7915 ACP	849-791-5P
P103		Program Mate Conn.		Cinch	DC37S	856-DC3-7S
		Hood		Cinch	DC24660	856-246-60
		Screw Clips		Cinch	D20419-0	109-204-19
P102		Sense Conn.		Cinch	DA-15S	856-DA1-5S
		Hood		Cinch	DA24658	856-246-58
		Screw Clips		Cinch	D20419-0	109-204-19
P101		Signal Conn.		Cinch	DA15P	856-DA1-5P
		Hood		Cinch	DA24658	856-246-58
		Screw Clips		Cinch	D20419-0	109-204-19

IEEE INTERFACE BOARD NO. 609-822-41

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER NAME	MANUFACTURER PART NUMBER	ELGAR PART NUMBER
C101	4.7 uF	Capacitor	35V	Sprague	196D475X0035JA1	823-475-61
C102,103,105,106	.005	Capacitor	10%	Centralab	DDM502	821-502-00
C104	33	Capacitor	25V	Sprague	196D336X0025PE4	823-336-51
CR102-106		Diode		T.I.	RC20GF331J	802-331-05
R101,102	330 ohm	Resistor	½W,5%	Speer	RC20GF331J	802-331-05
R103,107-111	3.3K	Resistor	½W,5%	Speer	RC20GF332J	802-332-05
R104	22K	Resistor	½W,5%	Speer	RC20GF223J	802-223-05
R112	100 ohm	Resistor	½W,5%	Speer	RC20GF101J	802-101-05
R113-115	100 ohm	Resistor	½W,5%	Speer	RC20GF101J	802-101-05
R116	1 K	Resistor	½W,5%	Speer	RC20GF102J	802-102-05
S101		Dip Switch		CTS	206-5	860-206-5X
U101-104		Quad Transceiver		Motorola	MC3446P	849-344-6X
U107,124		Hex Inverter		National	MC7404	849-740-4X
U106		Quad 2 Pos NAND		National	74132PC	849-741-32
U108		Quad 2 Pos NAND		National	7400PC	849-740-0X
U109		5 Bit Comparator		National	9324PC	849-932-4X
U110		13 INNAND		Fairchild	7465133	849-741-33
U111		8 Pos NAND		National	7430PC	849-743-0X
U112		Tri 3 Pos NAND		National	7410PC	849-741-0X
U113,114		Dual Schmidt Trig		National	7413PC	849-741-3X
U115,119		Quad 2 Pos AND		National	7408PC	849-740-8X
U116		Dual 4 Pos AND		National	7421PC	849-742-1X
U117		4-10 Line Dec.		National	7442PC	849-744-2X
U118		Lamp Driver		Fairchild	75461	849-754-61
U120-123		4 Bit Shift Reg.		National	7495PC	849-749-5X
U105		Hex Schmidt Trig.		National	7414PC	849-741-4X

POSITIVE TRUE LOGIC NO. 609-857-40

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C201	.1 uF	Capacitor	200V, 1%	Sprague	192P10492	822-104-05
R201	2.2K	Resistor	½W, 5%	Speer	RC20GF222J	802-222-05
U201,203,205,207		Quad 2-1 Select		National	DM74L157N	849-74L-15
U202,204,206		Hex Inverter		National	DM74L04N	849-74L-04

LOGIC BOARD NO. 609-821-42

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C201	.1 uF	Capacitor	200V, 10%	Sprague	192P10492	822-104-05
C202	4.7	Capacitor	35V	Sprague	196D475X0035JA1	823-475-61
CR201		Diode		T.I.	1N914	844-914-XX
R201	4.7K	Resistor	½W, 5%	Speer	RC20GF472J	802-472-05
U201		I.C.		National	SN74L10N	849-74L-10
U202-205		Quad 2-1 Select		National	DM74L157N	849-74L-15
U206-209		Quad Latch		National	DM74L75N	849-74L-75
LOGIC BOARD w/STORAGE 609-882-4X						
C201	.1 uF	Capacitor	200V, 10%	Sprague	192P10492	822-104-05
C202	4.7	Capacitor	35V	Sprague	196D475X0035JA1	823-475-61
CR201		Diode		T.I.	1N914	844-914-XX
R201	4.7K	Resistor	½W, 5%	Speer	RC20GF472J	802-472-05
U201		I.C.		National	SN74L10N	849-74L-10
U202-205		Quad 2-1 Select		National	DM74L157N	849-74L-15
U206-209		Quad Latch		National	DM74L75N	849-74L-75
U210-212		I.C.		National	DM74L04	849-74L-04

PHASE PROGRAMMER NO. 609-820-42

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C301-303	.1 uF	Capacitor	200V, 10%	Sprague	192P10492	822-104-05
R301,303,306,307, 309,310,311,312	10K	Resistor	1/8W, .25%	Dale	RN60C1002C	814-100-2C
U300,307-309		I.C.		RCA	CD4008AE	849-C40-08
U301		I.C.		National	LF356H	849-LF3-56
U302		Quad Op Amp			TL084CN	849-TL0-84
U303,304		I.C.		Ana. Devices	AD7531JN	849-753-1X
U305		PROM Sine			93448	849-SIN-48
U306		PROM Cosine			93448	849-COS-48
U311		OR Gate		RCA	CD4071AE	849-C40-71
U312,313		I.C.		RCA	CD4050AE	849-C40-50

RANGING SERVO NO. 609-855-42 (Two Inversion) - 609-871-42 (One Inversion)

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C401,402,403	1 uF	Capacitor	35V	Sprague	196D105X035JA1	823-105-61
C404	.0047 uF	Capacitor	200V, 10%	Sprague	192D47292	822-472-05
C405	10 uF	Capacitor	20V	Sprague	196D106X0020JA1	823-106-41
C406	47 pF	Capacitor	500V, 5%	Sangamo	DM15-470J	820-470-05
C407	.47 uF	Capacitor	200V, 5%	IMB	ZA2C474J	822-474-53
C408	1 uF	Capacitor	200V, 5%	IMB	ZA2C105J	822-105-53
CR401,402		Diode		T.I.	1N914	844-914-XX
R401,411,418	10K	Potentiometer		Spectrol	70Y103	819-103-30
R402,404,409,414-417,419,420,422	10K	Resistor	1/8W, 1%	Dale	RN60C1002F	813-100-2F
R403	100K	Resistor	½W, 5%	Speer	RC20GF104J	802-104-05
R407	1K	Resistor	½W, 5%	Speer	RC20GF102J	802-102-05
R408	13.3K	Resistor	1/8W, 1%	Dale	RN60C1332F	813-133-2F
R410	5.76K	Resistor	1/8W, 1%	Dale	RN60C5761F	813-576-1F
R412	20K	Resistor	1/8W, 1%	Dale	RN60C2002F	813-200-2F
R413	100K	Resistor	1/8W, 1%	Dale	RN60C1003F	813-100-3F
R421	2.4M	Resistor	½W, 5%	Speer	RC20GF245J	802-245-05
R423	10K	Resistor	½W, 5%	Speer	RC20GF103J	802-103-05
U401,404,405, 416-418		Op Amp		National	LF356	849-LF3-56
U402		Ana. Mult.		Burr Brown	4205J	849-420-5J
U403		A-D Converter		Ana. Devices	AD7531	849-753-1X
U406-408,411-413		4 Bit Full Adder		RCA	CD4008AE	849-C40-08
U409,414,421		Hex Inverter			DM74L04	849-74L-04
U410		OR Gate		RCA	CD4071AE	849-C40-71
U415		DAC		Burr Brown	DAC80 CB1-V	849-DAC-CB
U420		Ana. Switch		National	LF3331	849-133-31
R428	FSV					

150V SERVO No. 609-870-42

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C401,402,403	1 uF	Capacitor	35V	Sprague	196D105X035JA1	823-105-61
C404	.0047 uF	Capacitor	200V, 10%	Sprague	192P47292	822-472-05
C405	10 uF	Capacitor	20V	Sprague	196D106X0020JA1	823-106-41
C406	47 pF	Capacitor	500V, 5%	Sangamo	DM15-470J	820-470-05
C407	.47 uF	Capacitor	200V, 5%	IMB	ZA2C474J	822-474-53
C408	1 uF	Capacitor	200V, 5%	IMB	ZA2C105J	822-105-53
CR401,402		Diode		T.I.	1N914	844-914-XX
R401,411,418	10K	Potentiometer		Spectrol	70Y103	819-103-30
R402,404,408,409, 414-417,419,420, 422	10K	Resistor	1/8W, 1%	Dale	RN60C1002F	813-100-2F
R403	100K	Resistor	½W, 5%	Speer	RC20GF104J	802-104-05
R407	1K	Resistor	½W, 5%	Speer	RC20GF102J	802-102-05
R412	20K	Resistor	1/8W, 1%	Dale	RN60C2002F	813-200-2F
R413	100K	Resistor	1/8W, 1%	Dale	RN60C1003F	813-100-3F
R421	2.4M	Resistor	½W, 5%	Speer	RC20GF245J	802-245-05
R423	10K	Resistor	½W, 5%	Speer	RC20GF103J	802-103-05
U401,404,405, 416-418		Op Amp		National	LF356	849-LF3-56
U402		Ana. Mult.		Burr Brown	4205J	849-420-5J
U403		A-D Converter		Ana. Devices	AD7531JN	849-753-1X
U406-408,411-413		4 Bit Full Adder		RCA	CD4008AE	849-C40-08
U410		OR Gate		RCA	CD4071BE	849-C40-71
U414,421		Hex Inverter			DM74L04	849-74L-04
U415		DAC		Burr Brown	DAC80 CB1-V	849-DAC-CB
R428	FSV					

0-260V SERVO BOARD NO. 609-878-42

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C401,402,403	1 uF	Capacitor	35V	Sprague	196D105X035JA1	823-105-61
C404	.0047 uF	Capacitor	200V, 10%	Sprague	192P47292	822-472-05
C405	10 uF	Capacitor	20V	Sprague	196D106X0020JA1	823-106-41
C406	47 pF	Capacitor	500V, 5%	Sangamo	DM15-470J	820-470-05
C407	.47 uF	Capacitor	200V, 5%	IMB	ZA2C474J	822-474-53
CR401,402		Diode		T.I.	1N914	844-914-XX
R401,411,418	10K	Potentiometer		Bourns	3059Y	819-103-30
R402,404,409, 414-417,419, 420,422	10K	Resistor	1/8W, 1%	Dale	RN60C1002F	813-100-2F
R403	100K	Resistor	½W, 5%	Speer	RC20GF104J	802-104-05
R407	1K	Resistor	½W, 5%	Speer	RC20GF102J	802-102-05
R408	13.3K	Resistor	1/8W, 1%	Dale	RN60C1332F	813-133-2F
R412	20K	Resistor	1/8W, 1%	Dale	RN60C2002F	813-200-2F
R413	100K	Resistor	1/8W, 1%	Dale	RN60C1003F	813-100-3F
R421	2.4M	Resistor	½W, 5%	Speer	RC20GF245J	802-245-05
R423	10K	Resistor	½W, 5%	Speer	RC20GF103J	802-103-05
U401,404,405, 416,417,418		I.C.		National	LF356H	849-LF3-56
U402		Ana. Mult.		Burr Brown	4205J	849-420-5J
U403		I.C.		Ana. Devices	AD7531JN	849-753-1X
U406-408,411-413		I.C.		RCA	CD4008AE	849-C40-08
U410		I.C.		RCA	CD4071AE	849-C40-71
U414,421		Hex Inverter		National	DM74L04N	849-74L-04
U415		DAC		Burr Brown	DAC80-CBI-V	849-DAC-CB
R428	FSV					

VFO BOARD NO. 609-862-41

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C501,503,505,508, 509,512,519,520-524		Trim Capacitor				
C502,504	1000 pF	Capacitor	500V, 5%		DM15-102J	820-102-05
C506,510	.1	Capacitor	100V, 1%	IMB	BA1B104F	822-104-11
C507,511	.01	Capacitor	100V, 1%	IMB	BA1B103F	822-103-11
C513-515	.1	Capacitor	200V, 10%	Sprague	192P10492	822-104-05
C516,517	15-60 pF	Capacitor			538-006F-15-60	828-615-60
C518	15 pF	Capacitor	500V, 5%		DM15-150J	820-150-05
CR1-4		Diode		T.I.	1N914	844-914-XX
CR5		Zener Diode			1N821	843-821-XX
R502,508-511	10K	Resistor	1/8W, 1%	Dale	RN60C1002C	814-100-2C
R503	330K	Resistor	½W, 5%	Speer	RC20GF334J	802-334-05
R504	2.2K	Resistor	½W, 5%	Speer	RC20GF222J	802-222-05
R505	220 ohm	Resistor	½W, 5%	Speer	RC20GF221J	802-221-05
R506	11.5K	Resistor	1/8W, .25%	Dale	RN60C1152C	814-115-2C
R507	19.6K	Resistor	1/8W, 1%	Dale	RN60C1962F	813-196-2F
R512	100K	Resistor	1/8W, 1%	Dale	RN60C1003F	813-100-3F
R513	1K	Resistor	1/8W, 1%	Dale	RN60C1001F	813-100-1F
R514,515	47 ohm	Resistor	½W, 5%	Speer	RC20GF470J	802-470-05
U501		Quad Op Amp			TL084CN	849-TL0-84
U504,505		I.C.		National	LF356H	849-LF3-56
U506		I.C.			DG302	849-DG3-02
U507,511		I.C.		Ana. Devices	AD7531JN	849-753-1X
U508,509,512,513		I.C.		RCA	CD4008AE	849-C40-08
U510		I.C.		RCA	CD4071AE	849-C40-71
U514		I.C.		RCA	CD4001AE	849-C40-02
R501	9.31K	Resistor	¼W, 1%	Dale	RN60D9311F	815-931-1F
R516	715 ohm	Resistor	1/8W, 1%	Dale	RN60C7150F	813-715-0F
RT501	2K	Thermistor		Fenwel	PB32D1	818-PB3-2D

400 Hz OSCILLATOR NO. 609-859-40

SCHEMATIC DESIGNATION	VALUE	DESCRIPTION OR TYPE	RATING	MANUFACTURER		ELGAR PART NUMBER
				NAME	PART NUMBER	
C602	.02 uF	Capacitor			DDM203	821-203-00
C603,605	.33 uF	Capacitor	100V, 1%	IMB	BA1B334F	822-334-11
C604,606	.012 uF	Capacitor	100V, 1%	IMB	BA1B123F	822-123-11
C607,608,609	.047	Capacitor	100V, 1%	IMB	BA1B473F	822-473-11
C610,611,612	.1 uF	Capacitor	200V, 10%	Sprague	192P10492	822-104-05
CR601		Zener Diode			1N821	843-821-XX
Q601		Transistor			2N2222A	831-222-2A
R601	22K	Resistor	½W, 5%	Speer	RC20GF223J	802-223-05
R602,603,605	4.7K	Resistor	½W, 5%	Speer	RC20GF472J	802-472-05
R604	470	Resistor	½W, 5%	Speer	RC20GF471J	802-471-05
R606,611,616	10K	Resistor	½W, 5%	Speer	RC20GF103J	802-103-05
R607	1.2K	Resistor	½W, 5%	Speer	RC20GF122J	802-122-05
R608,613	10.7K	Resistor	1/8W, 1%	Dale	RN60C1072F	813-107-2F
R609,614	7.68K	Resistor	1/8W, 1%	Dale	RN60C7681F	813-768-1F
R610,615	5.23K	Resistor	1/8W, 1%	Dale	RN60C5231F	813-523-1F
R612	100K	Resistor	½W, 5%	Speer	RC20GF104J	802-104-05
R617-619,621,622, 625,626	10K	Resistor	1/8W, 1%	Dale	RN60C1002F	813-100-2F
R620,623,627	10K	Potentiometer		Spectrol	70Y103	819-103-30
R624,628	1K	Resistor	1/8W, 1%	Dale	RN60C1001F	813-100-1F
U601		Volt. Comparator			LM311	849-LM3-11
U603		I.C.			74LS92	849-74L-92
U604,605		Div. Counter			74L93	849-74L-93
U606-610		I.C.		National	LF356	849-LF3-56
Y601		Crystal	153.6KHz			864-153-R6

SECTION VII
DIAGRAMS

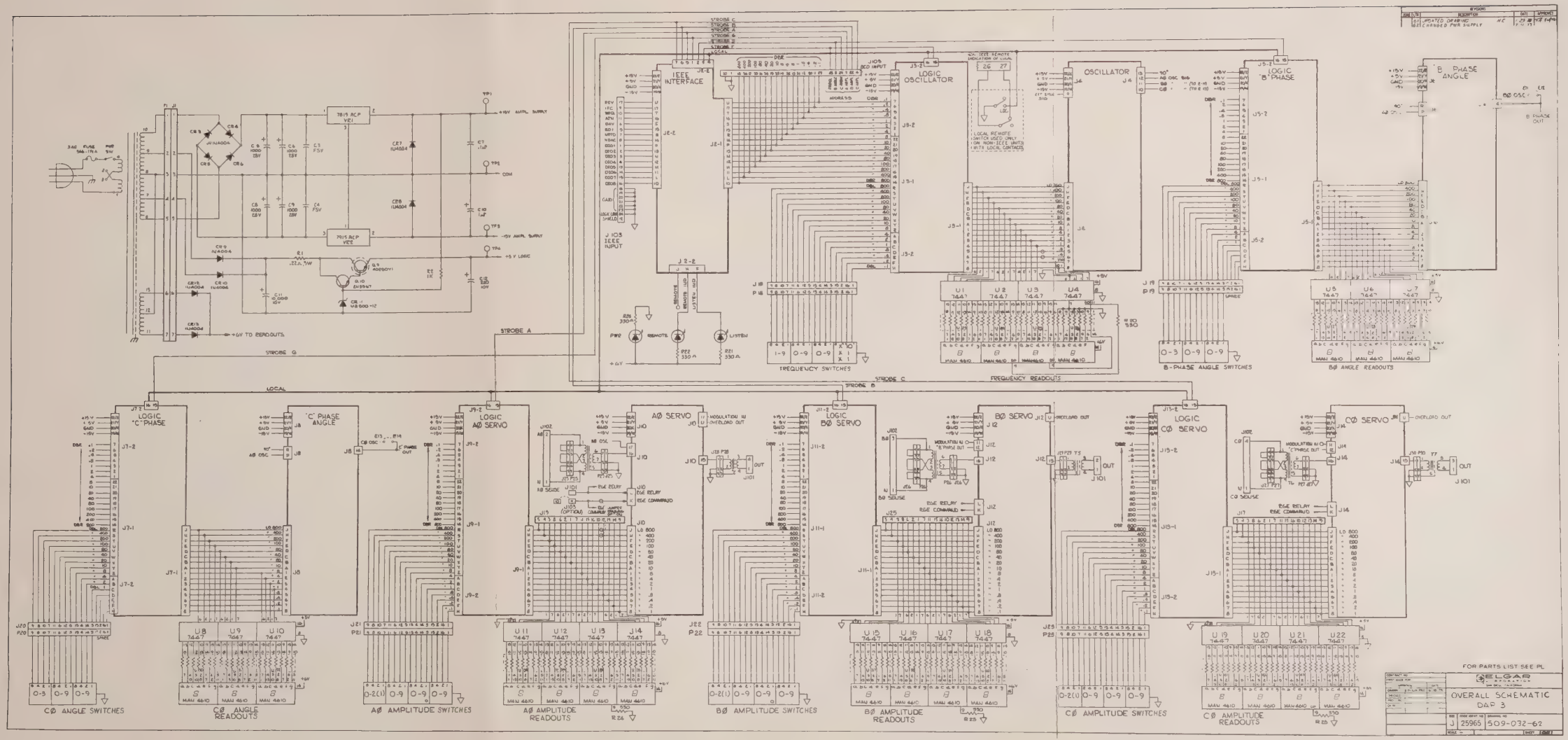


Figure 7.1. DAP Overall Schematic, 509-032-6X

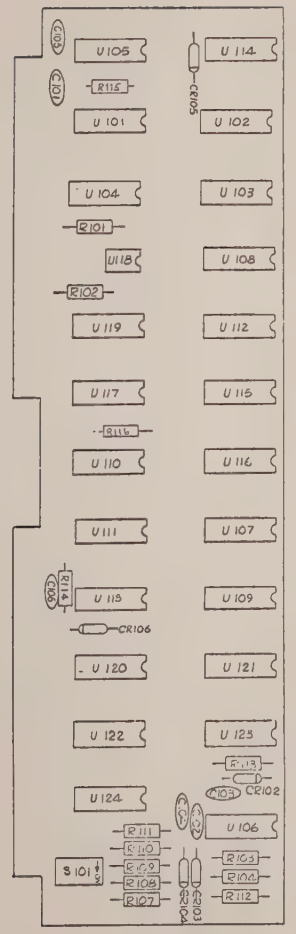


Figure 7.3. IEEE-488 Interface Parts Layout Drawing

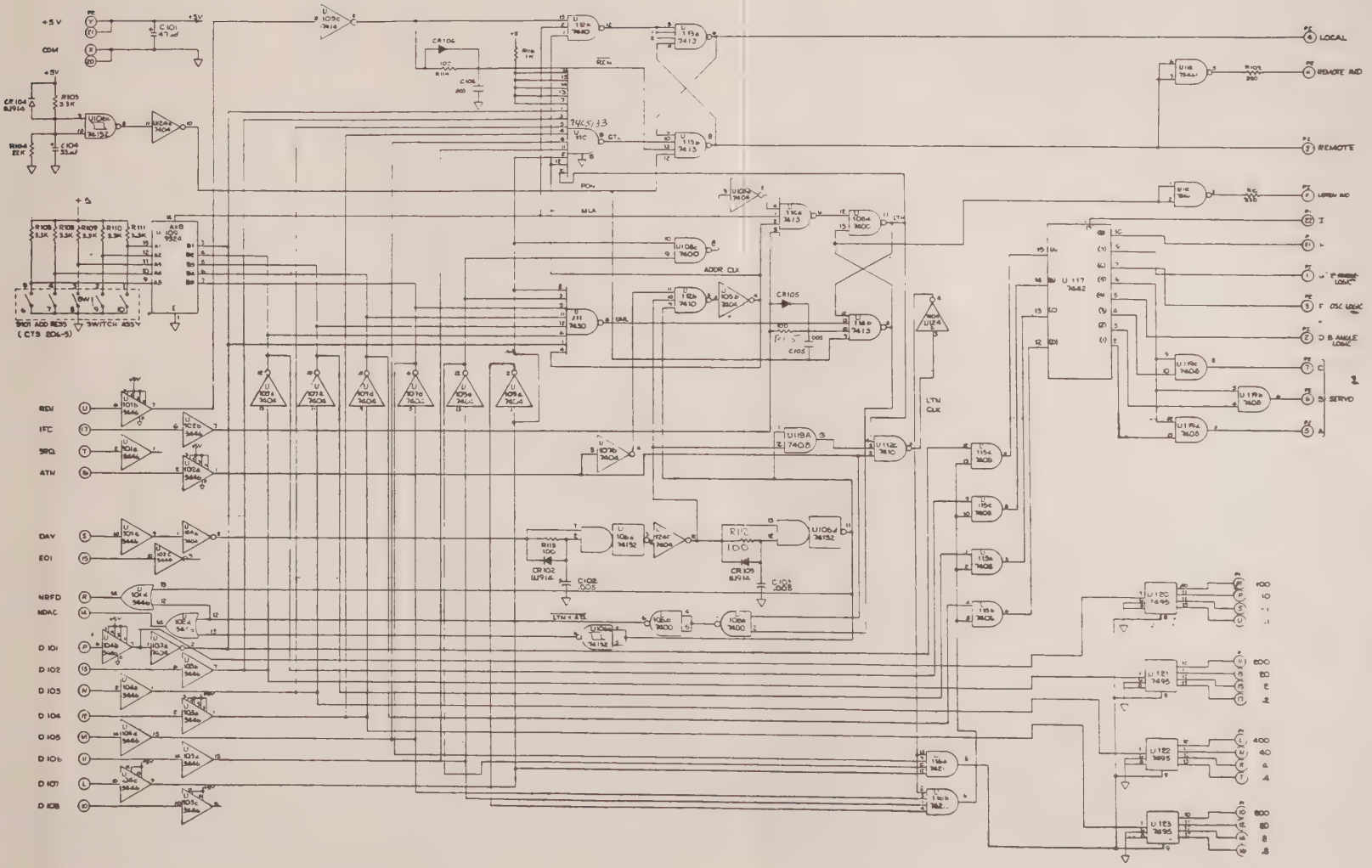


Figure 7.2. IEEE-488 Interface Board, 609-822-6X

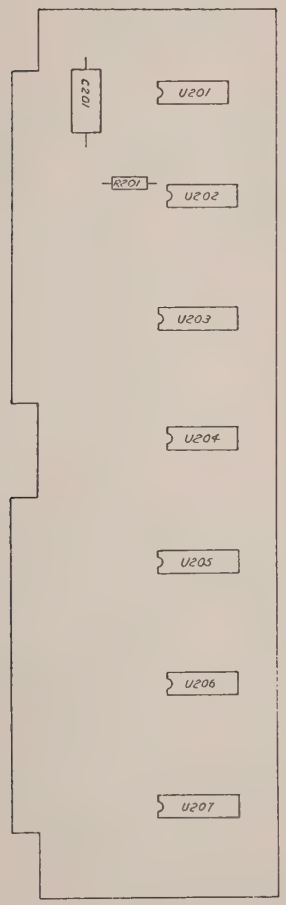


Figure 7.5. Positive True-No Storage Logic Board Parts Layout Drawing

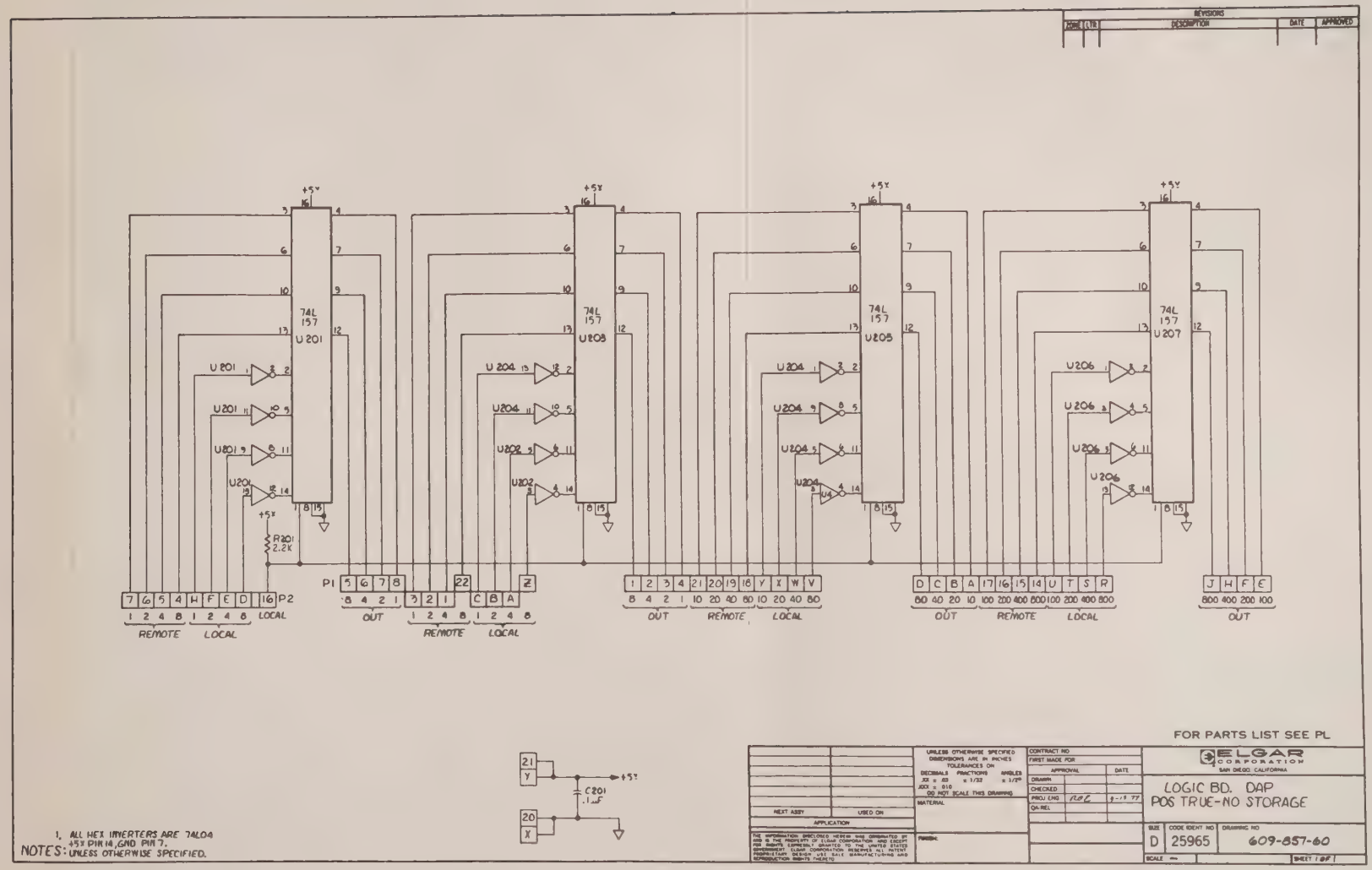


Figure 7.4. Positive True-No Storage Logic Board, 609-857-6X

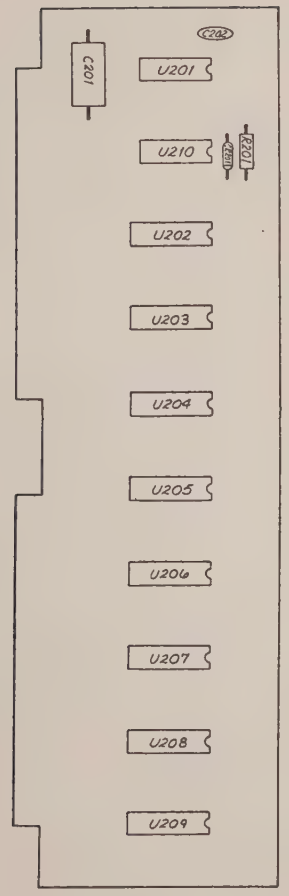


Figure 7.7. Storage Logic Board, Parts Layout Drawing

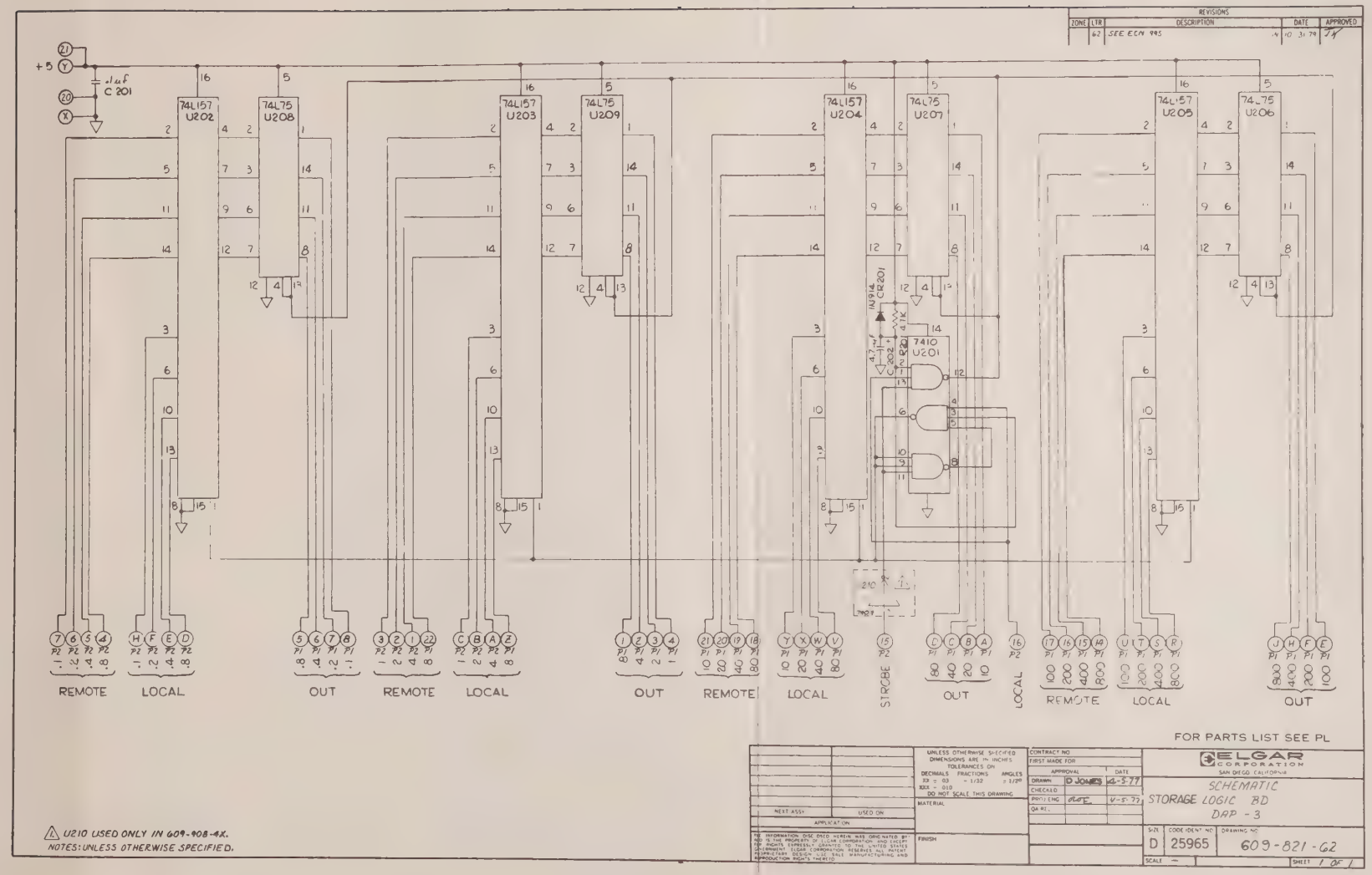


Figure 7.6. Storage Logic Board, 609-821-6X

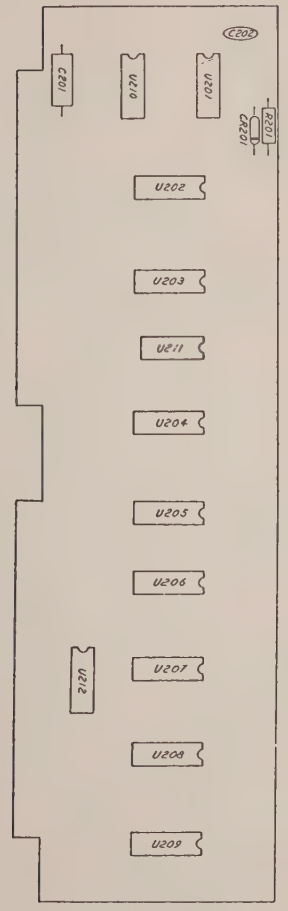


Figure 7.9. Positive True Logic Board, w/Storage, Parts Layout Drawing

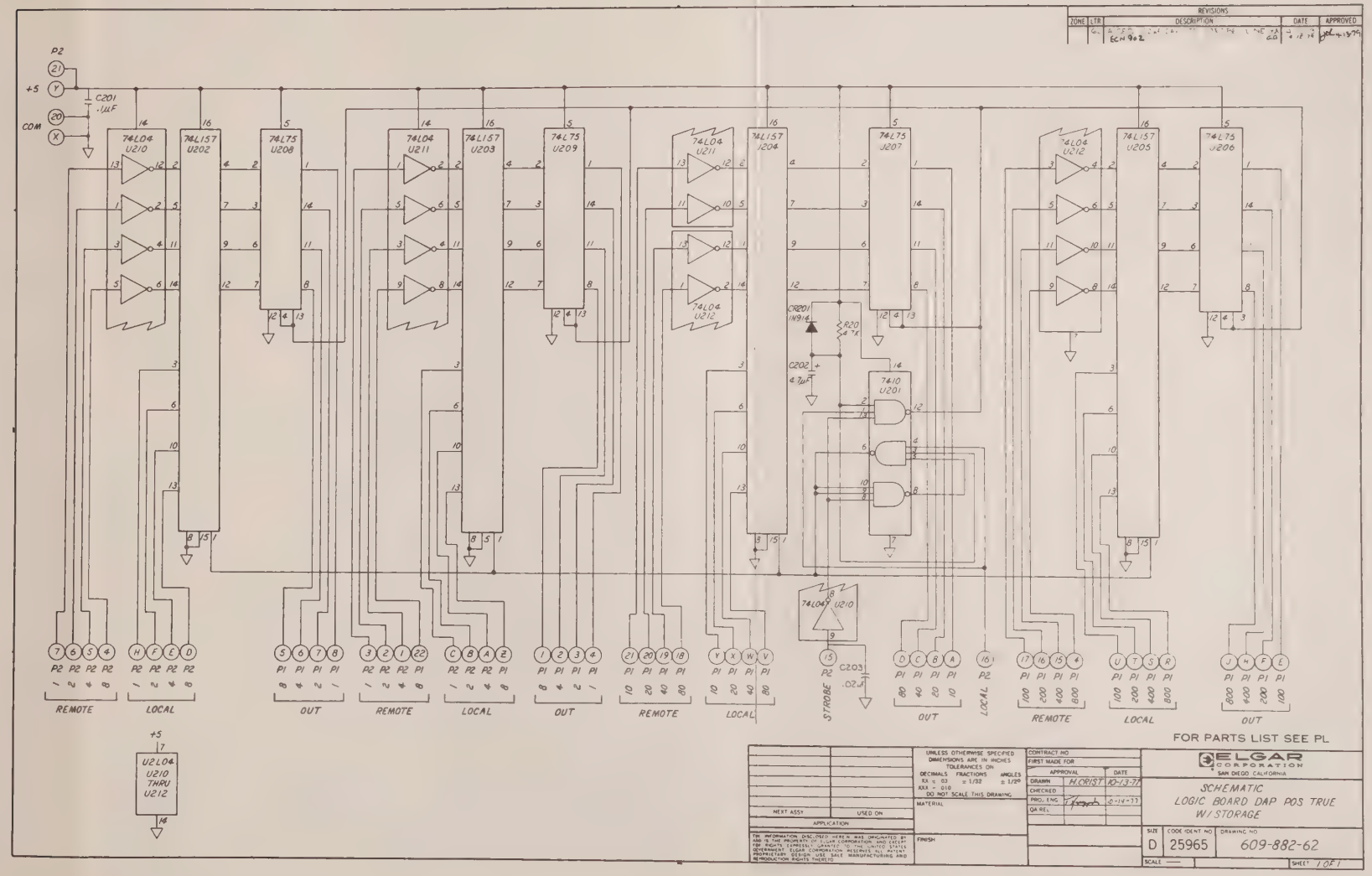


Figure 7.8. Positive True Logic Board, w/Storage, 609-882-6X

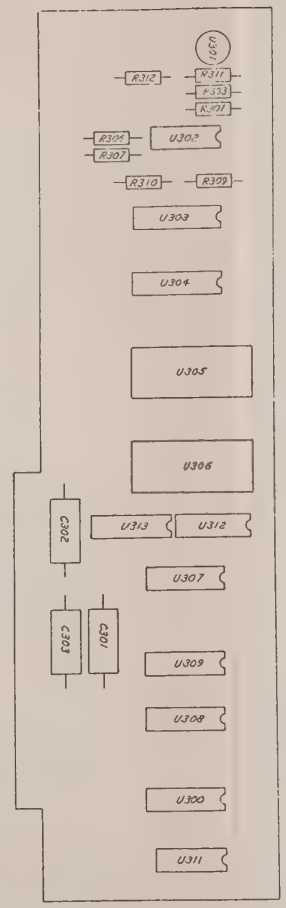


Figure 7.11. Phase Programmer, Parts Layout Drawing

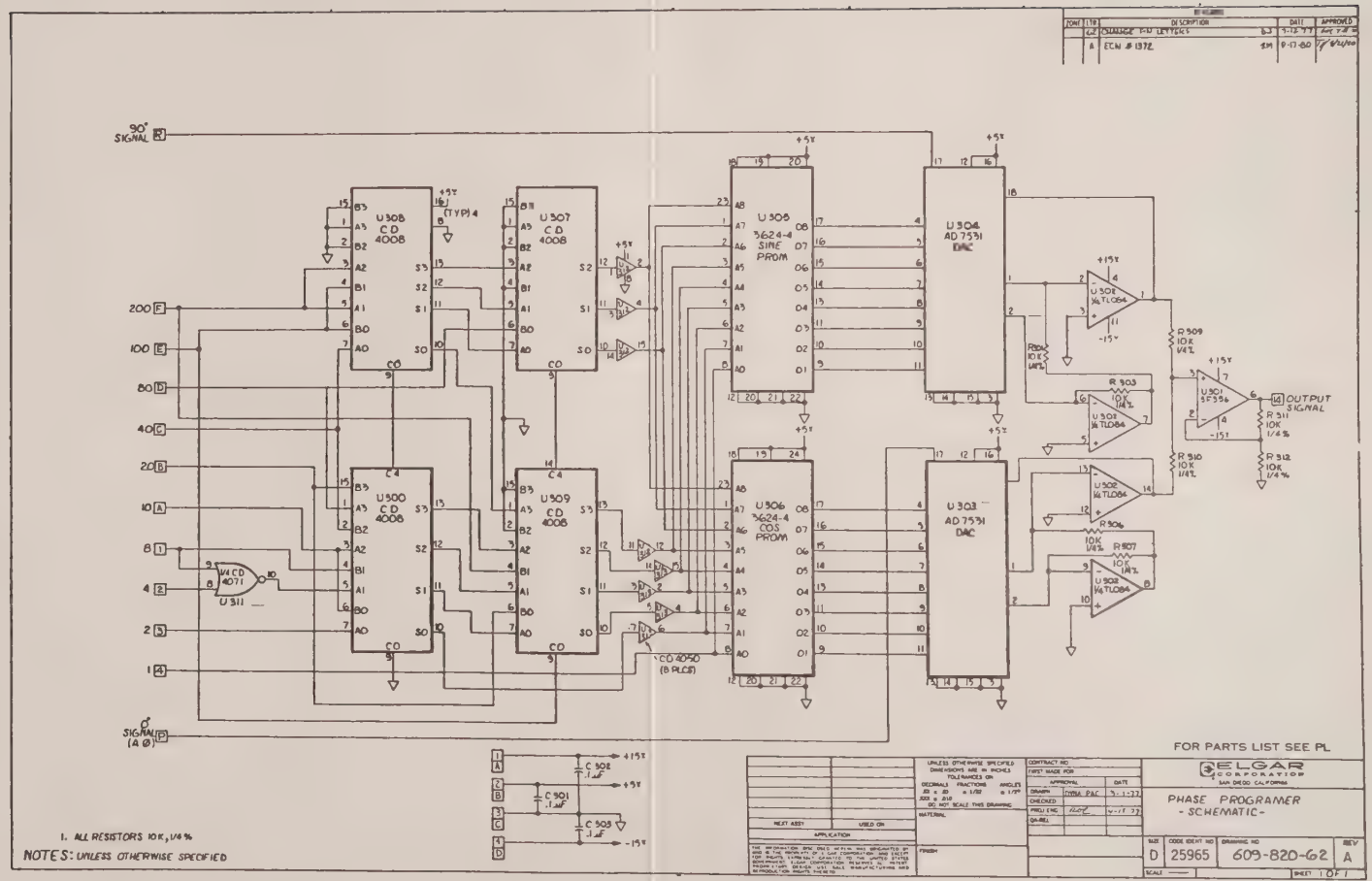


Figure 7.10. Phase Programmer, 609-820-6X

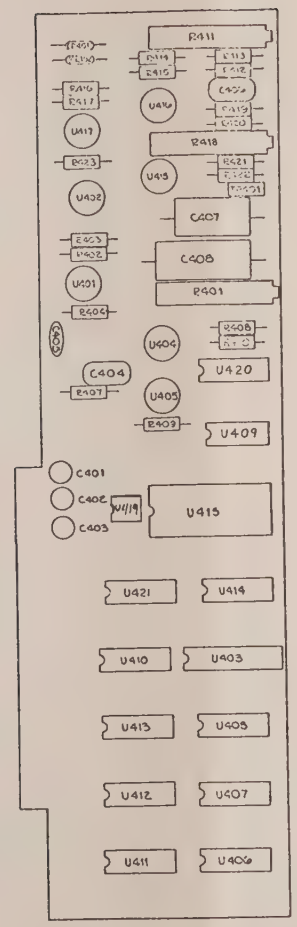


Figure 7.13. 130/260V Servo Board, Parts Layout Drawing

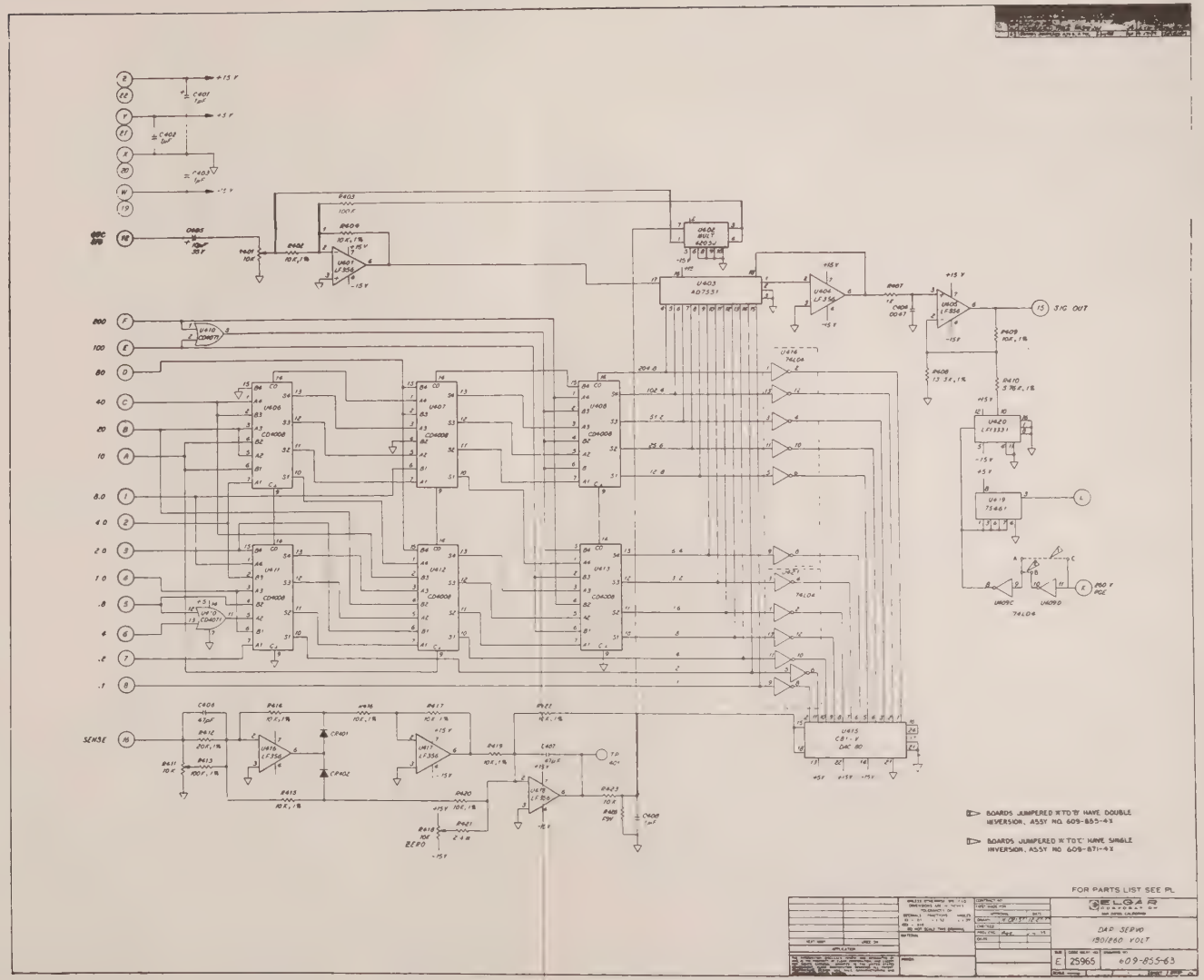

BOARDS JUMPERED 'A' TO 'B' HAVE DOUBLE INVERSION. ASSY NO. 609-855-63
BOARDS JUMPERED 'A' TO 'C' HAVE SINGLE INVERSION. ASSY NO 609-871-62
FOR PARTS LIST SEE PL
DAP SERVO
130/260 VOLT
E 25965
609-855-63

Figure 7-12. 130/260 Servo Board, 09-855-6X

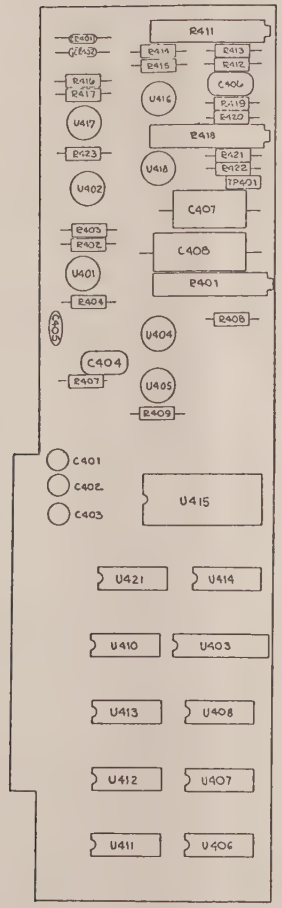


Figure 7.15. 150V Servo Board, Parts Layout Drawing

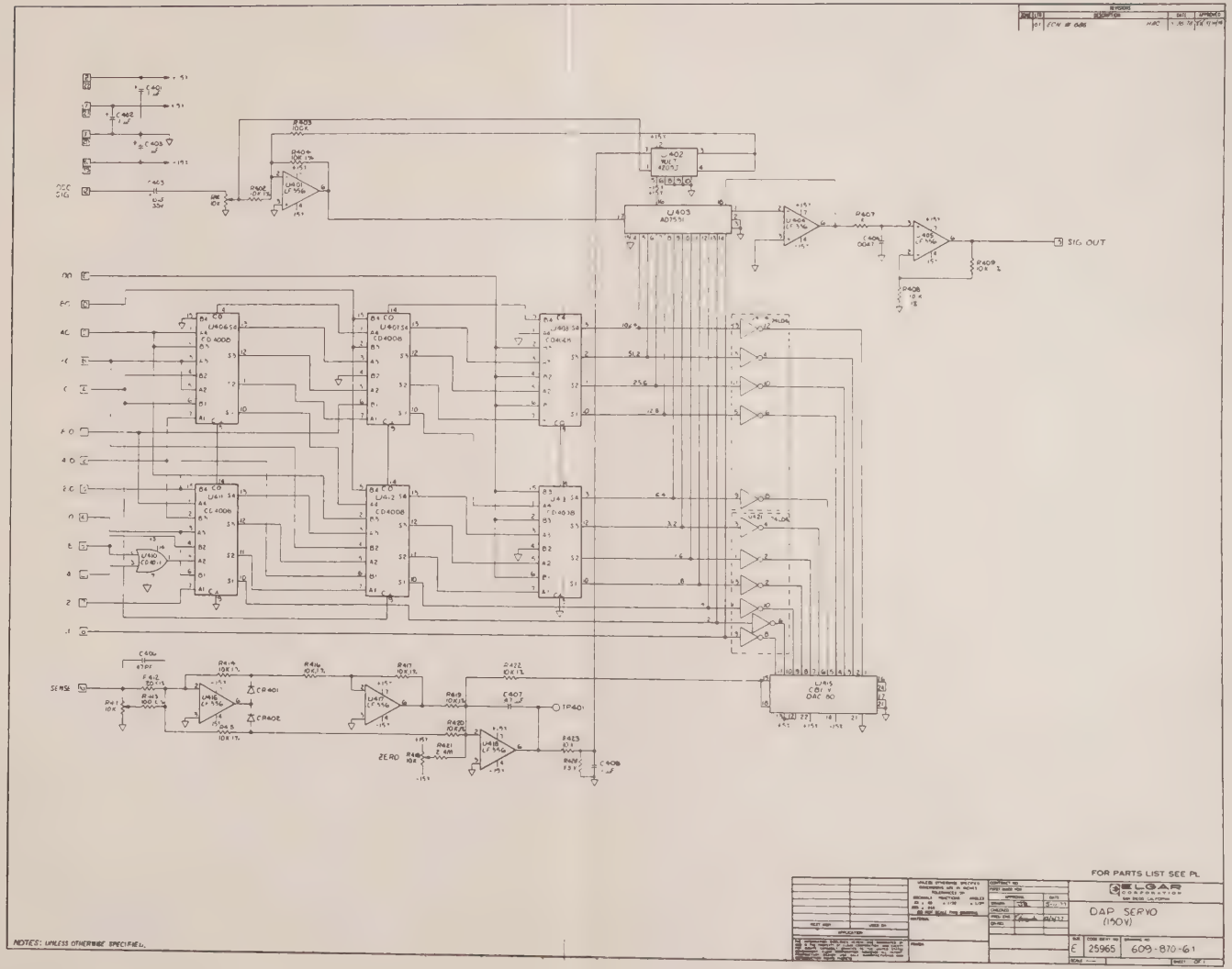


Figure 7.14. 150V Servo Board, 609-870-6X

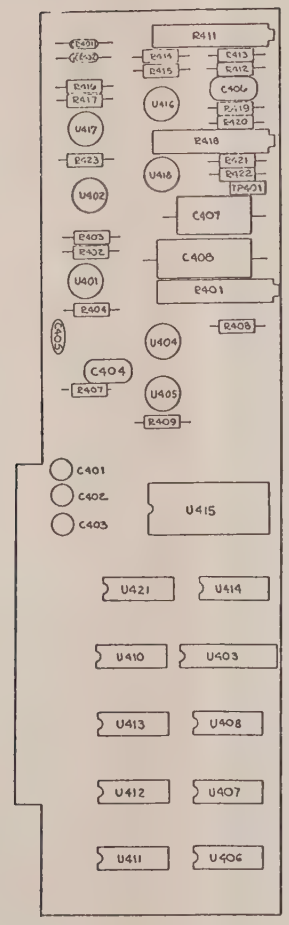


Figure 7.17. 0-260V Servo Board, Parts Layout Drawing

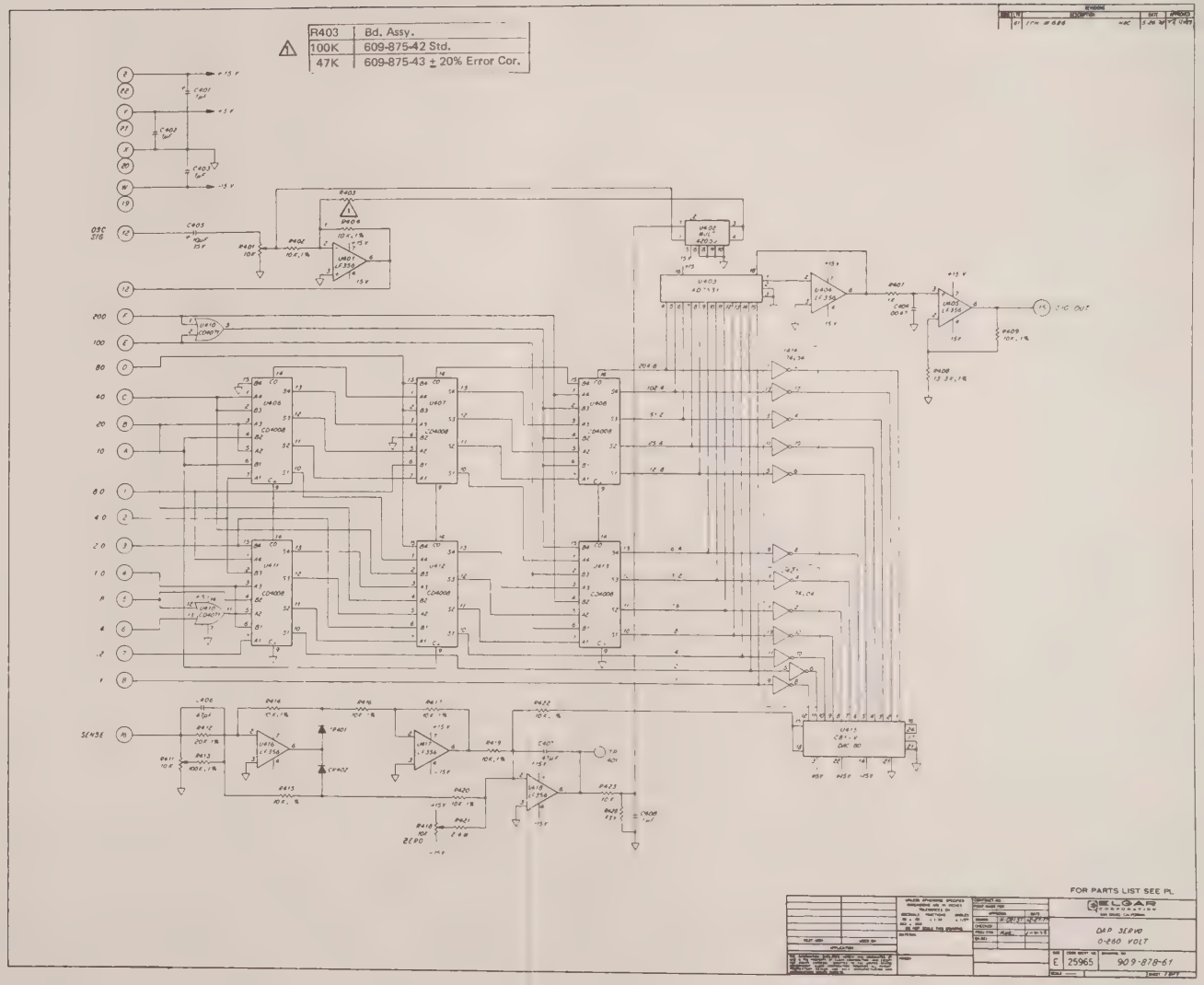


Figure 7.16. 0-260V Servo Board, 09-878-6X

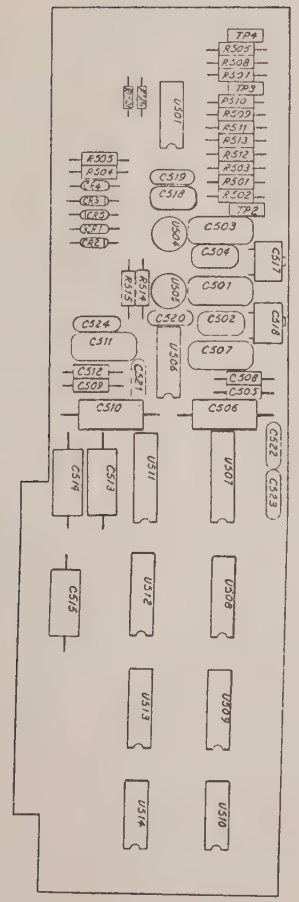


Figure 7.19. Programmable 3Ø Variable Frequency Oscillator, Parts Layout Drawing

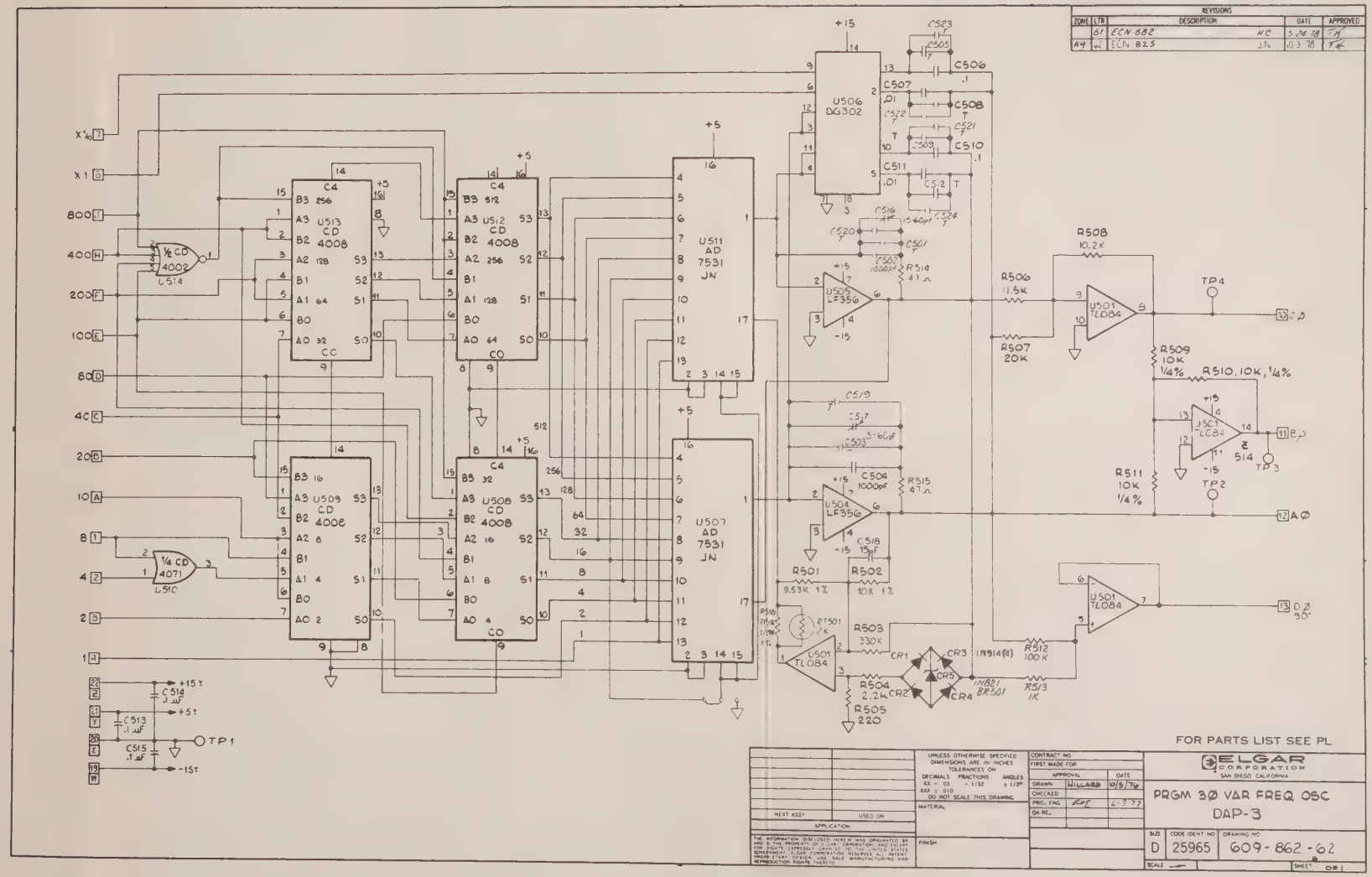


Figure 7.18. Programmable 3Ø Variable Frequency Oscillator, 609-862-6X

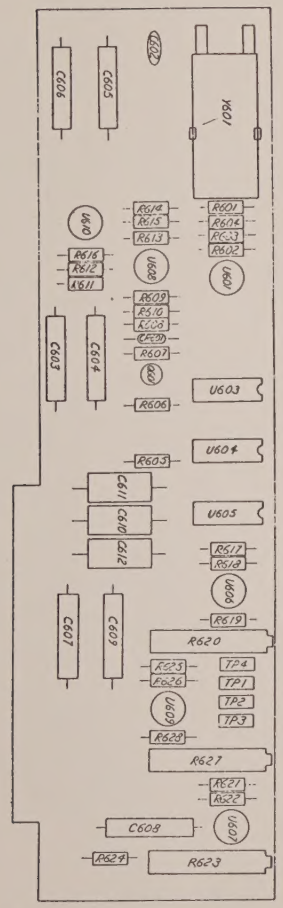


Figure 7.21. Fixed Frequency Oscillator, Parts Layout Drawing

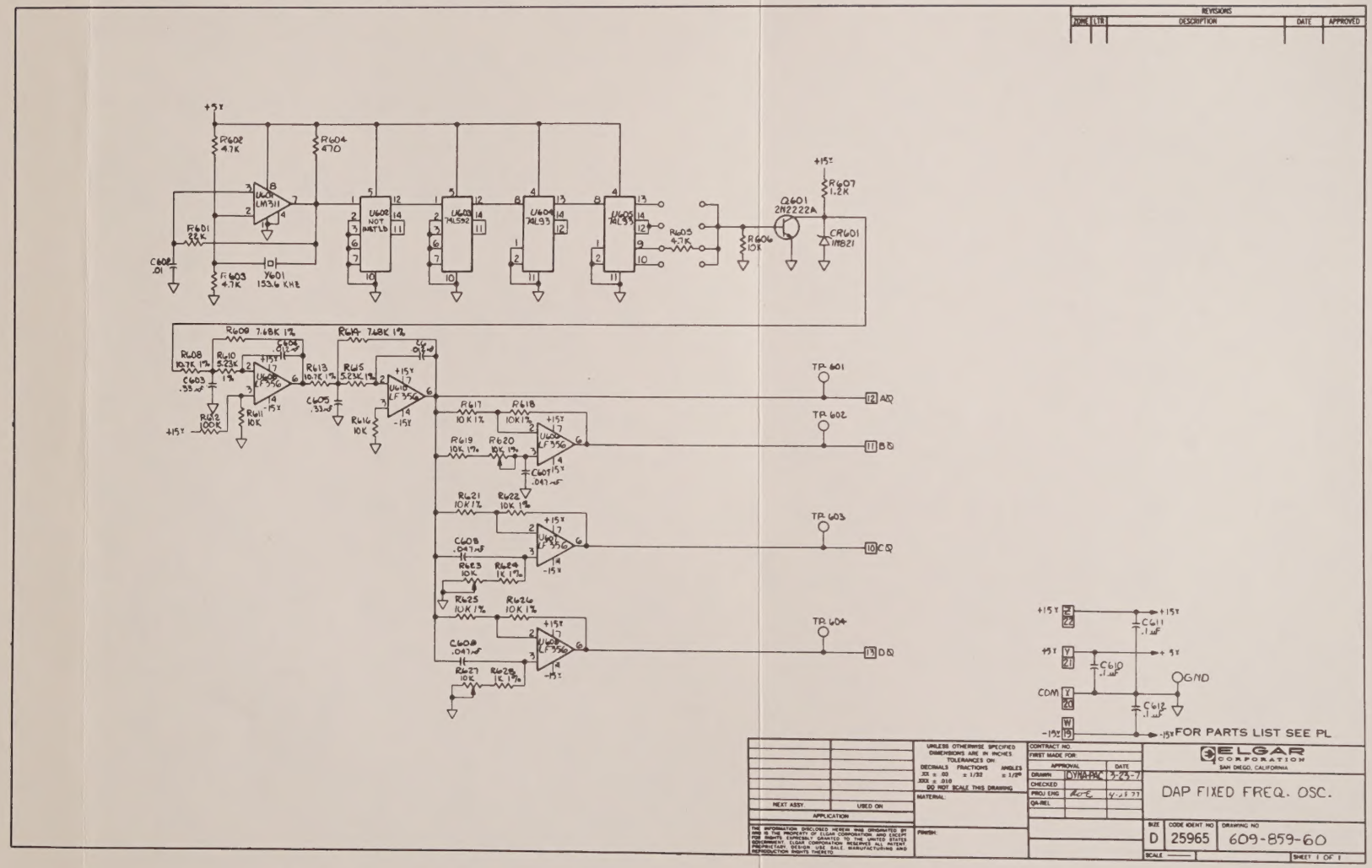


Figure 7.20. Fixed Frequency Oscillator, 609-859-6X

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